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Yield and performance enhancement of analog and mixed signal circuits

Yu Lin

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Yield and performance enhancement of analog and mixed signal circuits

by

Yu Lin

A dissertation submitted to the graduate faculty
in partial fulfillment of the requirements for the degree of

DOCTOR OF PHILOSOPHY

Major: Electrical Engineering

Program of Study Committee:
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Ames, Iowa

2006

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For the Major Program

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When I look back at myself about five years ago, I really did not know too much about VLSI and circuit design. Five years later, I am happily and proudly to see myself to obtain PhD degree in this area, which I never thought about before I came to Iowa State University.

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ABSTRACT

Parametric yield models for widely used area allocation schemes in ratio-critical analog circuits are developed in this dissertation. It is shown that some of the most widely used area allocation schemes are suboptimal and that significant improvements in parametric yield can be achieved with less intuitive area allocation approaches such as the optimal and near-optimal area allocation methods introduced in this work. Simulations and experimental results are presented which show quantitatively what improvements in yield can be achieved with improved area allocation strategies for resistive feedback amplifiers and R-2R DACs.

A strategy to optimize the power consumption in a class of digitally calibrated pipelined ADCs with a kT/C noise constraint is proposed. This optimization is based upon making tradeoffs between the kT/C noise budgeted in each stage, the number of stages, and the number of comparators in each stage. It is shown that significant reductions in total power consumption can be achieved with optimal noise distribution and bit/stage allocation.

Existing approaches for the design of interstage switched-capacitor amplifiers used in pipelined data converters have evolved following the notion that there are firm limits on input range and output range of the amplifier. In this dissertation, in contrast to existing approaches where the amplifier may be under-designed or over-designed in an attempt to meet a fixed signal swing window requirement, a method that enables the designer to select signal swing windows to provide acceptable levels of distortion is introduced. Following this approach, a new over-range protection scheme is developed which ensures that all residues of a given stage are mapped back into an acceptable distortion window of the following stages.

CHAPTER 1. GENERAL INTRODUCTION

In this dissertation, three works will be presented. The first work focuses on the yield enhancement strategy for ratio-critical analog circuits. The second and third work focuses on some design issues for energy efficient high-speed, high-resolution pipeline ADCs.

I. Yield Enhancement Strategy for Ratio-Critical Analog Circuits

A. Introduction

As we know, minimizing production cost is very important for a company. A low cost may mark the difference between success and failure. It is conjectured that for some circuits, the production cost, C , can be expressed as:

$$C = H \frac{A_1 + A_{\min}}{e^{-A_1 D}} \cdot \frac{1}{Y(A_1, \phi)} \approx H \frac{A_1 + A_{\min}}{Y(A_1, \phi)} \quad (1)$$

where H is some constant coefficient, A_1 is the effective area for the designed circuit, A_{\min} is some constant minimum area. The term $e^{-A_1 D}$ predicts the hard yield for a given circuitry, where D is the defects density. For a digital circuit with large area, this factor cannot be neglected. However, for analog circuit with small area, the factor is close to one. $Y(A_1, \phi)$ is the parametric yield of the designed function, which is a function of effective area A_1 and area allocation factor ϕ . Although only one ϕ is shown here, in practice, there may have several area allocation factors depending on the applications

In nowadays, with the decrease of the process feature size, the random variations of the process parameters are becoming more and more significant. It greatly affects the performance of the analog circuitry. For example, the large variations of the threshold

voltage, the sheet resistance, the contact resistance and etc. In practice, if a circuit's random variation exceeds the expectation, unless some form of calibration is incorporated, about the only way that most people will do is to increase yield by increasing the area. It is seldom realized that other factors such as the area allocation would also strongly affect the yield. Moreover, it is seldom realized that a high yield does not always guarantee low production cost.

One example is shown in Fig.1, where the parameter of interest is the resistance ratio of two resistors. This application has only one area allocation factor, which is the ratio of one resistor area and the total resistor area. For given accuracy, Fig.1(a) shows that for given area allocation scheme, the yield increase with the increase of the total resistor area. It also shows that there exists some optimal area allocation scheme, where for any given area, the yield with this optimal scheme is always better than other area allocation schemes. Fig.1(b) shows that when the area increases, the cost start to fall at beginning. After reaching some area, it starts to increase again with further increase of the area.

In this dissertation, the focus will be on optimizing the yield for fixed total resistor area by optimizing the area allocation for ratio-critical analog circuits, like R-2R DACs, resistive feedback amplifiers and resistor strings. For some of the applications, the issue of minimizing the production cost by optimizing both the area and area allocation could be addressed without too much extra work.

B. Contributions

Results show that quantitatively significant improvements in yield can be achieved with proposed optimal area allocation strategies for resistive feedback amplifiers and R-2R

DACs. It is also shown that the optimal area allocation scheme depends on the architectures of R-2R DACs. This work is the first report, which demonstrated that significant yield improvement could be obtained by appropriate area allocation between ratio-matched components for given total component area.

As mentioned above, people usually increase the area to improve the yield and did not recognize that changing the area allocation scheme will significantly affect the yield.

This work also point out that maximizing yield does not guarantee the lowest production cost, which most people did not realize.

II. kT/C Constrained Optimization of Power in Pipeline ADCs

A. Introduction

There is high demand for high-speed, high-resolution and lower power pipeline ADC [1-5]. It is widely used in many video and audio applications such as digital camera, cell phone, and laptops. For these kinds of portable applications, power dissipation is always of great concern.

However, pipeline ADC design strongly depends on applications. It involves many issues related to specific requirements such as integral nonlinearity (INL), signal to noise ratio (SNR), voltage supply, data conversion range, etc. Even for the same application, subtle architectural difference can cause dramatic impact on design requirements.

The number of bits per stage (BPS) and capacitor allocation are two important design parameters in pipeline ADCs. Lewis [1] examined the effects of the number of BPS on area and power. The author assumed that power ratio between the sample and hold amplifier (SHA) and comparator is constant. Based on this assumption, the author concluded that the

power dissipation would be minimized if the BPS is minimized. However, the assumption does not hold for different comparator and multiplying digital-to-analog converter (MDAC) architectures. As suggested by Cline [2], low resolution pipelines favors small BPS and slow capacitor scaling, which is defined as the capacitance ratio of the previous stage and the following stage, and high resolution pipelines favors large BPS and rapid capacitor scaling. However, the approximation of linear relationship between the total capacitance and the total power is crude. Goes [6] studied several design examples and concluded that the conventional wisdom of using the smallest possible BPS only applied to ADC with less than 10-bit resolution. Later on, Kwok [7] investigated the optimal BPS dependency of the power ratio of SHA to comparator for ADC to optimize power. It was suggested that for power ratio of SHA and comparator less than 20, the optimal BPS is around 2 with one bit redundancy. If the ratio is within 20~100, the optimal BPS will be 3 with one bit redundancy. For the same power ratio, high-resolution pipelined ADCs favor low BPS, which conflicts with the conclusion drawn by Cline [2]. Kwok also scaled the stage resolution to optimize the power. If the total resolution of the ADC changes, the optimal combination of BPSs may change, which indicate that the results may not be applicable to ADCs with different resolutions.

In this dissertation, a strategy to optimize the power consumption in a class of digitally calibrated pipelined ADCs with a kT/C noise constraint is proposed. Optimal BPS and capacitor scaling function will be determined.

B. Contributions

This optimization of power is based upon making tradeoffs between the kT/C noise budgeted in each stage, the number of stages, and the number of comparators in each stage.

It is shown that significant reductions in total power consumption can be achieved with optimal noise distribution and bit/stage allocation.

III. New Over-range Protection Scheme in Pipelined Data Converters

A. Introduction

The presence of uncompensated nonlinearities in the signal path can significantly degrade the performance of a pipeline analog to digital converter (ADC). Few of these nonlinearities contribute to recoverable errors whereas other results in non-recoverable errors. Both recoverable errors and non-recoverable errors limit the performance of most pipelined data converters. Excessive growth in the residue path caused by nonlinearities will cause such recoverable or non-recoverable errors. In particular, the concern is that the residue can cause the output of one or more amplifier stages to saturate. These excessive signals are often termed over-range signals. Modifications of the basic amplifier structure are included in some pipeline ADCs [3,8,9] to limit the over-range signals. The circuits that provide this over-range protection are generally termed an over-range protection circuits.

Existing approaches for the design of interstage switched-capacitor amplifiers used in pipelined data converters have evolved following the notion that there are firm limits on input range and output range of the amplifier. This results in excessive design requirements of a pipeline ADC. In this dissertation, a new over-range protection scheme based on these signal swing windows and critical points will be investigated to achieve a relaxed pipeline ADC design.

B. Contributions

In this work, it is recognized that the limits on signal swing are not dictated by binary and somewhat arbitrary boundaries but rather by increasing levels of distortion with signal swing. The concept of defining a series of signal swing windows based on the degree of distortion present in the gain stage amplifier is formalized. A set of "critical points" on the transfer characteristics are identified that are useful for determining robustness of any given over-range protection circuit. In contrast to existing approaches where the amplifier may be under-designed or over-designed in an attempt to meet a fixed signal swing window requirement, the designer can select signal swing windows to provide acceptable levels of distortion. Following this approach, a new over-range protection scheme is developed which ensures that all residues of a given stage are mapped back into an acceptable distortion window of the following stage.

IV. Dissertation Organizations

The dissertation follows the journal paper format, which consists of seven chapters. Chapter 1 contains the general introduction. In Chapter 2, the yield enhancement area allocation strategy of R-2R ladder is developed, which was published in Kluwer Journal of Analog Integrated Circuits and Signal Processing, Nov. 2003. In this chapter, the R-2R ladder is used in binary-weighted current R-2R DAC. The results show that the yield of R-2R DACs satisfying certain INL requirement can be significantly improved with the proposed optimal area allocation strategy. In Chapter 3, yield enhancement strategy with optimal area allocation for ratio-critical analog circuits will be developed. This paper was published in IEEE transactions on Circuits and Systems-I, March 2006. In this chapter, three different

architectures of resistive feedback amplifiers will be investigated. The yield of equal-current R-2R DAC will be discussed in details. The resistor string will also be investigated. The results show that the yield of resistive feedback amplifier and the equal-current R-2R DAC can be significantly improved compared to conventional area allocation schemes. It will also be proved that the conventional area allocation scheme for resistor string is already optimal. In Chapter 4, experimental results for resistive feedback amplifiers and equal-current R-2R DAC will be presented. In Chapter 5, a strategy to minimize the total power consumption for pipeline ADC with kT/C noise constraint will be presented. In Chapter 6, a new over-range protection scheme in pipelined ADC will be presented. Chapter 7 contains the general conclusions.

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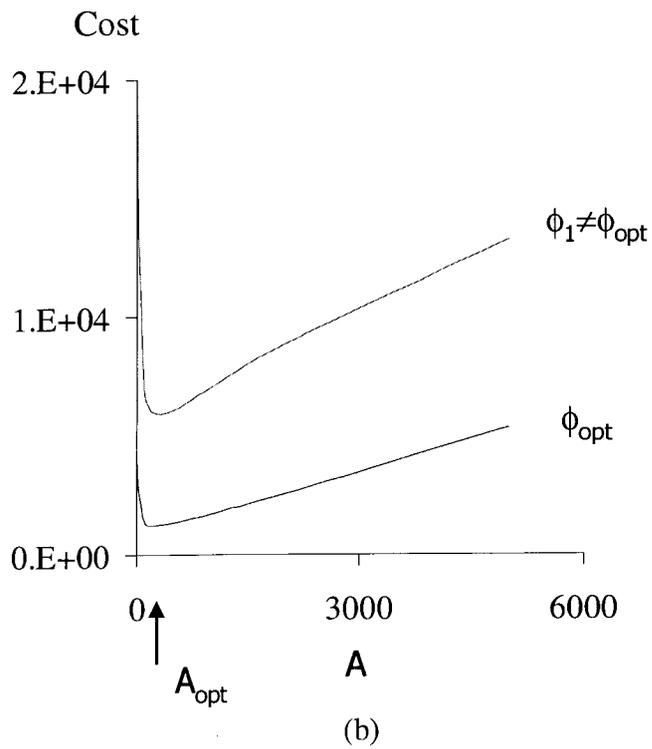
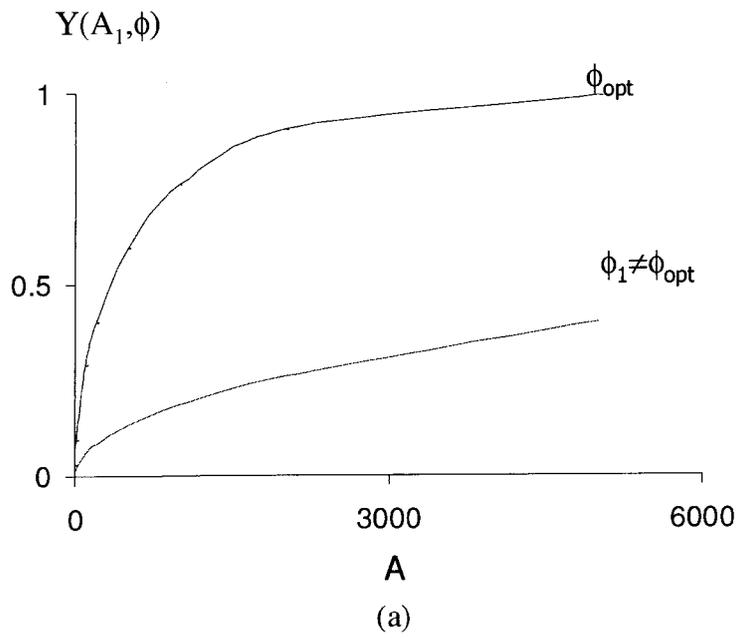


Fig.1 (a) Yield and (b) cost of accurate resistance ratio

CHAPTER 2. AREA ALLOCATION STRATEGIES FOR ENHANCING YIELD OF R-2R LADDERS

A paper published in *The Journal of Analog Integrated Circuits and Signal Processing*

Yu Lin and Randall Geiger

Abstract

A new strategy for allocating area, at layout, for enhancing the soft yield of R-2R ladders is introduced. In contrast to the conventional and convenient approach of allocating equal area to each R/2R bit-slice, the new strategy allocates progressively larger areas to higher-order bits. With this strategy, the INL yield for a fixed total resistor area as determined by local random variations in the sheet resistance is optimized. Simulation results show that the new area allocation strategy provides significant improvements in INL yield compared to what is achievable with the conventional area allocation strategy.

I. Introduction

It is well recognized that different layout approaches of a given circuitry may result in significantly different soft yields. Because of the importance of layout, considerable effort has been focused on optimizing the layout of matching-critical circuits. However, most of this work has been concentrated on the matching of two nominally identical devices or on arrays of nominally identical devices. Invariably, reported results are based upon using a standard cell and are concerned about placement and segmentation strategies for reducing yield loss due to random parameter variations. Little attention has been paid to circuits

which require ratio matching where the ratio is not equal to one and essentially no consideration has been given to the issue of area allocation between components when the precise value of some components in a circuit is more critical than the value of others. In this work, the issue of optimal area allocation between the resistors in R-2R ladders is addressed.

Gradients and local random variations in the sheet resistance are the two major factors that contribute to ratio-matching errors in resistors. The effects of first or higher-order gradient effects on ratio matching can be minimized by appropriate placement, segmentation and common-centroiding of the layout [1-3]. If the types of gradient effects present can be accurately modeled, these techniques can be used to drive the gradient effects to arbitrarily low levels. If gradient effects have been taken care of, local random sheet resistance variations become the dominant contributor to ratio errors. Several researchers have reported that the standard deviation of the resistance or capacitance in integrated devices due to local random variations [4, 5] is inversely proportional to the square root of the area used for the components. Thus, the conventional strategy for minimizing the effects of random local variations in the sheet resistance is to allocate sufficient area to the matching-critical components to achieve acceptable matching performance. Unfortunately, there is little in the literature to suggest how area relates to yield when the ideal component ratios are not unity. As a result, many engineers either allocate excessive area to achieve an acceptable yield or suffer a yield penalty if inadequate area is allocated. Unfortunately, too, is the observation that many engineers do not know whether they have allocated too much or too little area for a given yield target until after test results have been obtained and, if the yield is inadequate, they often do not know whether the yield loss is due to inadequate area

allocation or other factors. Although it might appear that allocating excessive area is a viable design strategy, aside from the increased die costs and hard yield loss associated with the excessive area allocation, the increased parasitic capacitances associated with the extra area will invariably limit high-frequency performance of the circuit.

Beyond the issue of area allocation is the area partitioning and this has received little, if any, attention in the literature. Invariably, if an $n:1$ component ratio is required, it is assumed that this will require an $n:1$ area ratio as well. Thus, the conventional area partitioning strategy can be termed a component-ratio strategy. Whether the component-ratio area partitioning strategy is optimal deserves consideration. As a consequence, the problem of soft-yield management in ratio-critical circuits becomes one of determining how to optimally allocate and partition area between the matching-critical components.

One partial solution to this problem is to develop better tools or analytical procedures for area allocation so that area can be judiciously allocated for achieving a desired yield. It was recently shown that for some applications requiring two or more ratio-matched components the yield can be significantly improved [6] by using an area partitioning strategy different from the standard component-ratio strategy. Thus, a second part of a solution to this problem is to develop better area partitioning strategies for ratio-critical circuits.

In the following, we will concentrate on the linearity of R-2R ladders by studying specifically the INL of these structures. We will develop an analytical procedure for predicting the soft yield based upon the areas allocated to the individual resistors in the structure. We will also introduce a new area partitioning strategy that will improve yield for a given total area. In these discussions, it will be assumed that appropriate segmentation and placement is used to render gradient effects non-dominant.

A simple example shows the important role that the area partitioning plays in these structures. Consider the case of the n-bit R-2R ladder DAC of Fig.1 where the resistors without a subscript are nominally of value R and those with the ‘2’ subscript are nominally of value 2R. It will be shown that by using the new area partitioning strategy for resistor layout, the standard deviation of the INL for a 16-bit DAC will be reduced by 48% when compared to that attained with the standard component-ratio area partitioning strategy. This same example can be viewed in a different way. If the standard area partitioning strategy was used along with the area needed to obtain a yield of 81.5%, it will be shown that the new area partitioning strategy will improve the yield to 99% for the same total area.

II. Area-Partitioning

If the gradient effects are neglected, it is well-known that the standard deviation of the normalized resistance of any rectangular resistors of length L and width W due to local random variations in the sheet resistance can be expressed as [6]:

$$\frac{\sigma_{R_{ran}}}{R_N} = \frac{A_p}{\rho_N \sqrt{WL}} = \frac{A_p}{\rho_N \sqrt{A_R}} = \frac{K_p}{\sqrt{A_R}} \quad (1)$$

where A_p is a process parameter that characterizes the random local sheet resistance variation, ρ_N is the nominal value of the sheet resistance, and A_R is the area of the resistor. For convenience, the ratio of A_p to ρ_N is denoted as K_p .

The two standard area partitioning approaches depicted in Fig. 2 for implementing an R-2R ladder can be both termed component-ratio partitioning strategies. In this figure, the switches d_1, \dots, d_n are not shown. We term strategy of Fig. 2(a) the “conventional series” strategy. In the conventional series strategy, the “R” resistors are all implemented with a unit

resistor cell and the “2R” resistors are implemented with two of the unit resistor cells connected in series. The second, depicted in Fig. 2 (b) is termed the “conventional parallel” strategy. In the latter, the “2R” resistors are all implemented with the standard resistor cell and the “R” resistors are implemented with two standard resistor cells placed in parallel.

For the n-bit R-2R DAC depicted in Fig. 1, we will assume the amplifier and the feedback resistor are ideal. This DAC has $N = 2^n$ output levels and from the definition of the endpoint INL [7], it can be readily shown that the INL at the k^{th} output is given by:

$$INL_k = \left(\sum_{i=1}^n d_i I_i - \frac{k}{N-1} \sum_{i=1}^n I_i \right) / I_{NOM} \quad 0 \leq k \leq N-1 \quad (2)$$

where the sequence $\langle d_i \rangle$ is the digital input, k is the decimal equivalent of $\langle d_i \rangle$, I_i is the current flowing in the corresponding bit resistors and the I_{NOM} is the nominal current of one LSB. The INL is defined to be the maximum of the absolute values of the INL_k and is formally expressed as:

$$INL = \max_{0 \leq k \leq N-1} \{ |INL_k| \} \quad (3)$$

The standard deviation of the INL is denoted by σ_{INL} . The INL is a random variable and is the N^{th} order statistic of the N correlated random variables, $|INL_k|$ $0 \leq k \leq N-1$. Analytical expressions for statistics of the INL such as σ_{INL} are not mathematically tractable. This information is, however, essential for soft yield prediction and computer simulations can be used for characterizing the INL.

A comparison of the standard deviation of the INL for the conventional n-bit series and the conventional n-bit parallel area partitioning strategies for the R-2R ladder will now be made. For this comparison, it will be assumed that the total area for the R-2R ladders is

fixed for all n and that the standard deviation of a resistor with this total area is 0.1% of the nominal value. A C-program was used for a statistical analysis of the resultant R-2R ladders and the results are shown in Fig.3. From this plot, it is apparent that for a fixed total resistor area, the conventional series layout will give a substantial improvement in yield when compared with the conventional parallel layout. It can be deduced that to enhance yield, it is better to allocate more area to the “2R” resistors than to the “R” resistors. From this example, it is apparent that area allocation plays an important role in yield. This example naturally raises two questions: What is the optimal area allocation between the “R” and “2R” resistors and how should the area be allocated between more significant and less significant bit slices for a given total area? In what follows we will attempt to answer these two questions and develop insight into what resistors play the most important role in the overall INL.

With reference to Fig. 1, it can be shown analytically that the standard deviation of the INL_k , σ_{INLk} is a maximum at $k = 2^{n-1}$ and at $k = 2^{n-1}-1$. This can be expressed as:

$$\max(\sigma_{INLk}) = \sigma_{INL(2^{n-1})} = \sigma_{INL(2^{n-1}-1)} \quad (4)$$

It is instructive to identify the major contributors to $\max(\sigma_{INLk})$. Although a formal expression of $\sigma_{INL(2^{n-1})}$ for any n is possible, the expression for the case where $n = 3$ does provide the desired insight. If we assume each resistor can be expressed as the sum of a nominal value and a random component, $R = R_{NOM} + R_r$, it follows from a tedious but straightforward derivation for a 3-bit R-2R ladder that

$$\max(\sigma_{INLk}) = \sigma \left\{ \frac{4}{7} \left(\frac{3 R(0)_r}{16 R_{NOM}} + \frac{3 R(1)_r}{16 R_{NOM}} - \frac{5 R_2(1)_r}{16 R_{NOM}} - \frac{1 R(2)_r}{4 R_{NOM}} - \frac{3 R_2(2)_r}{4 R_{NOM}} - \frac{R(3)_r}{R_{NOM}} + \frac{3 R_2(3)_r}{2 R_{NOM}} \right) \right\} \quad (5)$$

From this expression, it is apparent that the MSB resistors $R(3)$ and $R_2(3)$ provide the largest contributions to the standard deviation. These two resistors comprise the MSB bit slice of the R-2R ladder. Further, within the bit slice, the resistor $R_2(3)$ is a bigger contributor to the overall standard deviation than the resistor $R(3)$. This indicates the “2R” resistor is a larger contributor to $\sigma_{INL(2^{n-1})}$ than the “R” resistor in the bit-slice supporting the earlier observation that the “standard series” configuration which allocates more area to the “2R” resistors should have a lower $\sigma_{INL(2^{n-1})}$ than the “standard parallel” configuration. This can be generalized to suggest that the MSB resistors make a larger contribution to the standard deviation of the $\max(\sigma_{INLk})$ than the LSB resistors and the “2R” resistors make a larger contribution than the “R” resistors in arbitrary R-2R ladder networks. Although $\max(\sigma_{INLk})$ is not the standard deviation of the INL, this expression gives insight into the roles that different resistors play in determining the overall INL. Intuitively, the overall INL should be reduced if the standard deviation of those resistors that make the individual INL_k s large can be reduced. This can be achieved if more area is allocated to the MSB resistors and less area is allocated to the LSB resistors while keeping the total area constant and even further improvements can be made if more area is allocated to the “2R” resistors than to the “R” resistors. Of course, if too much area were removed from the LSB resistors, the contributions of these resistors to the overall INL would again dominate thus deteriorating the INL. Although this qualitative discussion provides guidance into how the area should be allocated, a more rigorous investigation is needed to determine how the area should be optimally allocated between resistors in the R-2R structure. An n-bit R-2R structure is comprised of $(2n+1)$ resistors and thus the key question is how to allocate area between these $(2n+1)$

elements. This $(2n+1)$ variable optimization problem itself is quite involved. It can be argued, however, that a near optimal solution can be obtained by considering how to distribute area between bit slices and how to allocate area within a bit slice. This facilitates a major reduction in the order of the optimization problem. In what follows, we will first consider a two-parameter optimization [7] and then extend it to a three-parameter optimization.

A. Two-Parameter Optimization

We will consider an 8-bit R-2R ladder but the results extend to R-2R ladders of any order. Referring again to Fig. 1, observe each bit slice has an “R” resistor and a “2R” resistor allocated to the slice. The area allocated to these two resistors will be designated as the area associated with that slice (bit). The area allocated to the p^{th} bit will be denoted as A_p . Therefore, the first slice area is A_1 , the second is A_2 , and the MSB slice area is A_n for an n -bit ladder. For convenience, we will allocate the termination resistor, $R(0)$ in Fig. 1, to the LSB slice. In each slice, the allocation of area between the “R” resistor and the “2R” resistor must also be determined. Denote the ratio of the area allocated to the “2R” resistor and the “R” resistor in the p^{th} bit as k_p . An optimal area assignment strategy involves determining the optimal values of A_1, \dots, A_n and k_1, \dots, k_n . With $2n$ variables and only one constraint, the total area, an analytical formulation of the optimal area allocation algorithm appears unwieldy.

To reduce the order, we will assume that the area ratio of the neighboring slices is m , i.e. $A_2 = mA_1, A_3 = mA_2, \dots, A_n = mA_{n-1}$ and the area ratio of the 2R and R resistor inside each slice is k as depicted in Fig.4. We have thus reduced a $(2n-1)$ variable optimization

problem to the 2-variable optimization problem of finding optimal values for m and k . With this order reduction, for a given fixed A_{total} , the standard deviation of the INL of the ladder is only a function of k , m . For relative comparisons, the value of A_{total} is arbitrary. For an 8-bit R-2R ladder, we first assumed $k = 2$ (this corresponds to the “conventional series” strategy discussed earlier) and then varied m by computer simulations to find a minimum in the standard deviation of the INL. We found a shallow one-dimensional local minimum in the INL around $m = 1.7$ as depicted in Fig. 5. Then m was fixed at 1.7 and k was varied to obtain an optimal value of k and the optimal value of k around $k = 2.2$ as depicted in Fig. 6 was obtained. This one-dimensional local minimum was even shallower. We then repeated this procedure, fixing first k and then m but saw little further movement in either k or m . It can thus be concluded that the two-dimensional local minimum is shallow and approximately given by $m=1.7$ and $k = 2.2$. From these simulations, it is apparent that the standard deviation is somewhat more sensitive to m than to k for $n = 8$. Simulations were undertaken for values of n larger and smaller than $n = 8$. The local minima did not change much from the values of $m=1.7$ and $k = 2.2$.

Although the local minimum is quite shallow, it should be observed that the value of $m = 1.7$ is far from the value of $m = 1$ that would correspond to one of the standard component-ratio area partitioning strategies thus indicating much more area should be allocated to the higher-order bit slices than to the lower-order bit slices.

B. Three-Parameter Optimization

In the two parameters optimization procedure, we allocated the area for the extra termination resistor to the LSB slice and did not allow the area partitioning within a bit slice

to change with slice location. These restrictions can be altered by considering a three-parameter optimization, which is still quite manageable. The parameters m_1 , m_2 and k_1 are defined respectively as the area ratio of the adjacent “2R” resistors, the area ratio of the adjacent “R” resistors and the area ratio of all of the “2R” resistors to that of all of the “R” resistors. For convenience, the LSB terminating resistor that is in series with the LSB “R” resistor is treated as the final “2R” resistor and is designated as $R_2(0)$. Formally,

$$m_1 = \frac{A_{R_2(k)}}{A_{R_2(k-1)}} \quad \text{for } n \leq k \leq 1$$

$$m_2 = \frac{A_{R(k)}}{A_{R(k-1)}} \quad \text{for } n \leq k \leq 3$$

$$k_1 = \frac{\sum_{i=0}^n A_{R_2(i)}}{\sum_{i=2}^n A_{R(i)}}$$

This area partitioning is depicted in Fig.7. Following a simulation strategy similar to that used in the two-parameter case, the optimal values of $m_1 = 1.7$, $m_2 = 1.7$ and $k_1 = 2.2$ were obtained. With the exception of the area associated with the termination resistor, these results are essentially the same as obtained in the two-parameter optimization and these results are essentially independent of n .

Although the two-parameter and the three-parameter optimizations do not necessarily provide the same local minimum as the completely general $(2n-1)$ parameter optimization, they do suggest that a substantially higher percentage of the total area needs to be allocated to the higher-order bits than to the lower-order bits. As such, it is unlikely that the more general $(2n-1)$ parameter optimization would result in substantive improvements over what was obtained with the much simpler two-parameter optimization.

C. Simplified Area Allocation Strategy

Since the local minimums obtained above are quite shallow, near optimal INL performance can be obtained even if the area allocations differ modestly from the optimal. This will make the layout more practical. However, maintaining the area ratios for the lower order bits will become increasingly challenging since the areas for the lower-order slices are becoming quite small. Since the area for the lower-order slices is quite small and comprises only a few percent of the total area for large n , the question naturally arises: Can the LSB slices have the same area to reduce the layout efforts? Since this non-optimal area assignment will cause degradation in the standard deviation of the INL, the increase in INL will be considered.

Table 1 gives the increase in the standard deviation of the INL for selected resolution R-2R ladders over what would be obtained if the same total area were used with optimal area partitioning. In this table, s is the number of LSB stages with the same area. The first $(n-s+1)$ stages were designed with the $m = 1.7$ and $k = 2.2$ area allocation strategy and the area in the last s stages were all equal to the area in stage s . The increase in the standard deviation of the INL, σ_{INL} , is less than 1% for the cases considered. For example, if the last 8 stages of a 16-bit R-2R network all have the same area, the penalty in σ_{INL} over what would be obtained with optimal area allocation is less than 1%.

Table 1. The standard deviation of R-2R ladder

n	s	σ_{INL}
8	3	0.5445%
10	4	0.6819%
12	5	0.6445%
14	6	0.5302%
16	8	0.9915%

D. Comparison with Existing Strategies

The new area allocation performance based upon $m = 1.7$ and $k = 2.2$ is compared with that of the conventional series and the conventional parallel approaches in Fig.8 for different values of n . In this plot, the standard deviation of the INL was normalized to that of the standard parallel layout to facilitate the comparison. From this plot, it is apparent that the standard deviation is reduced more with higher ladder resolution. For a 3-bit R-2R ladder, the decrease in the standard deviation is 25% and for a 16-bit R-2R ladder it is about 60% relative to what is attainable with the conventional parallel layout that allocated equal area to each bit.

The normalized sigma INLs for the three different approaches discussed above are compared in Fig.9. The data of the simplified approach is based upon the area assignments given in Table 1. From these simulation results, it is apparent that the three different approaches give almost the same σ_{INL} and consequent the same yield.

III. Yield Enhancement with Optimal Area Allocation

The improvement in the standard deviation of the INL over what is achievable with a standard equal area/slice area allocation strategy was presented in the previous section. What is of bigger concern is how much improvement in yield can be obtained with the optimal area allocation strategy. The yield improvement will be discussed in this section.

The soft yield [6] of a device that has a single random error mechanism that is normally distributed can be expressed as:

$$Y = erf\left(\frac{\epsilon}{\sigma\sqrt{2}}\right) \quad (6)$$

where, ε is the tolerable error in a parameter of interest, σ is the standard deviation of the same parameter, and $\text{erf}(x)$ is the standard error function. If Y_1 is the yield for a standard deviation σ_1 , it is easy to show that the yield Y_2 if the standard deviation is changed to σ_2 relates to Y_1 by the relationship

$$Y_2 = \text{erf}\left(\frac{\sigma_1}{\sigma_2} \text{erf}^{-1}(Y_1)\right) \quad (7)$$

From (7), if σ_1 is the optimal standard deviation (σ_{\min}) and Y_1 is the corresponding optimal yield (Y_{opt}), it follows that the yield for a non-optimal sigma, Y , is given by

$$Y = \text{erf}\left(\frac{\sigma_{\min}}{\sigma} \text{erf}^{-1}(Y_{\text{opt}})\right) \quad (8)$$

It follows from (8) that a comparison of the optimal yield with a conventional series and a conventional parallel area assignment can be made from the data in Fig. 8. This comparison is made in Fig. 10. In this comparison, the total area for the optimal area assignment for each n was selected to obtain a yield of 99% with the optimal area assignment. From this comparison, it is apparent that a substantial yield penalty will be paid if the optimal area allocation strategy is not used. For example, if the area is determined so that the optimal yield of a 16-bit R-2R ladder is 99%, then the conventional series area allocation approach would result in a yield of only 81.5%. Stated alternately, if a conventional series area allocation had a soft yield due to random variations in the sheet resistance of 81.5%, then the new area allocation strategy would provide a yield of 99% with the same total area allocated to the R-2R ladder.

The concepts presented here can be extended to the optimal allocation of area in capacitors and transistors in related applications.

IV. Layout of Standard Cells

It is still important to use a standard cell and, if gradients are a problem, common centroid layouts of the R-2R array. With the required scaling of area between slices, the issue of how the ratios of $m = 1.7$ and $k = 2.2$ can be achieved deserves attention. Since the local minimums are reasonably shallow, there is considerable flexibility in the layout. One possible standard cell layout that involves rationing in the first 6 stages and that then maintains a constant area per slice will now be described. Assume the “2R” resistor of the MSB block is comprised of 288 unit cells arranged 12 wide and 24 long. The MSB “R” resistor would then be 12 wide and 12 long. The next MSB block would have a “2R” resistor that is 9 wide and 18 long and the corresponding “R” resistor would be 9 wide and 9 long. The third MSB block would have the “2R” resistors 7 wide by 14 long and the corresponding “R” resistor would be 7 wide by 7 long. The fourth “2R” resistor would be 5 wide by 10 long and the corresponding “R” resistor would be 5 wide by 5 long. The next “2R” resistor would be 4 wide by 8 long and the corresponding “R” resistor would be 4 wide by 4 long. All remaining slices would have “2R” resistors that are 3 wide by 6 long and all “R” resistors that are 3 wide by 3 long. In this case, the sequence of m values is 1.78, 1.65, 1.96, 1.56, 1.78, 1, 1, ..., 0.75 and the sequence of k values are all 2. Applying this approach to an 8-bit R-2R ladder, the increase in the standard deviation of the INL, σ_{INL} , is only 0.9% of the INL achievable with the optimal approach. Therefore, a modest deviation from the optimal k and m values will still give a near-optimal yield. Other layout strategies that use the standard cell and which may provide closer agreement to the $m = 1.7$ and $k = 2.2$ area allocation strategy exist as well.

In the formulation presented in this paper, the issues of contact resistance and edge definition were not addressed. The random component of the contact resistance does play a significant role in yield prediction of R-2R networks but it can be shown that the contact resistance does not alter the area allocation results developed in this paper. The randomness of the edges of the resistors will play a role as well when a large number of unit cells are used to realize the resistors in the R-2R network. A formulation for the optimization of area allocation when both sheet resistance variations and edge variations are contributors to yield loss is straightforward but quite tedious and is not included in this work.

V. Conclusions

An assessment of the INL yield associated with random variations in the sheet resistance for the standard series and standard parallel equal bit/slice area layouts of an R-2R ladder was made. This assessment shows that the yield of the standard series layout was somewhat better than the yield for the standard parallel layout. A new method for distributing area between the resistors of different bit slices has been introduced that provides near optimal yield for a given total resistor area. This area allocation strategy results in placing a higher percentage of the total area in the higher-order bit slices than in the lower-order bit slices.

The optimal area allocation strategy provides a substantial improvement in soft yield when compared to what is achievable with the standard equal area allocation strategies.

Acknowledgement

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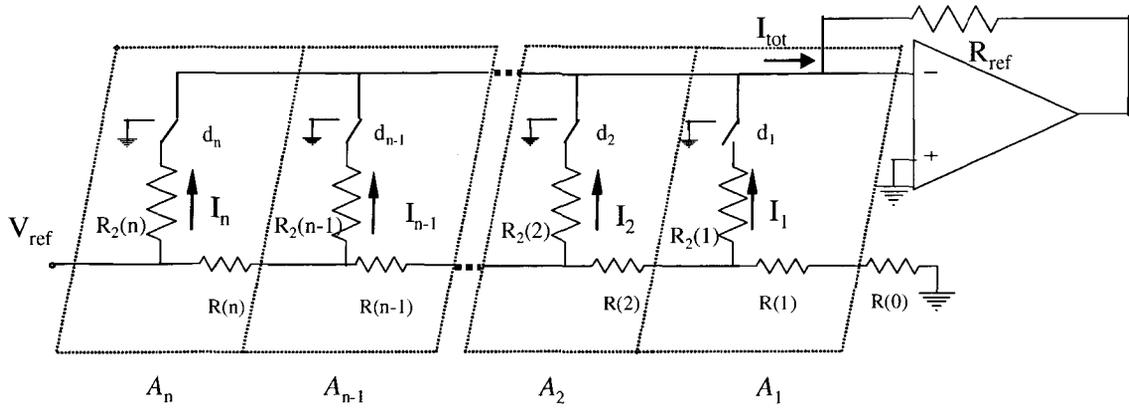


Fig.1. A basic n-bit R-2R DAC

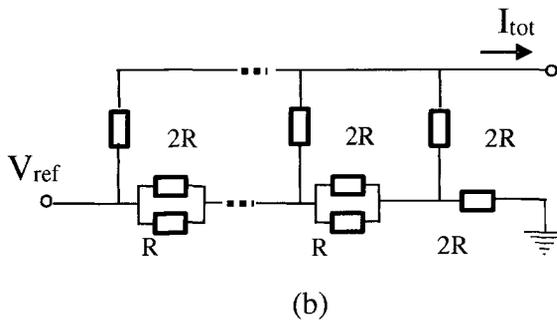
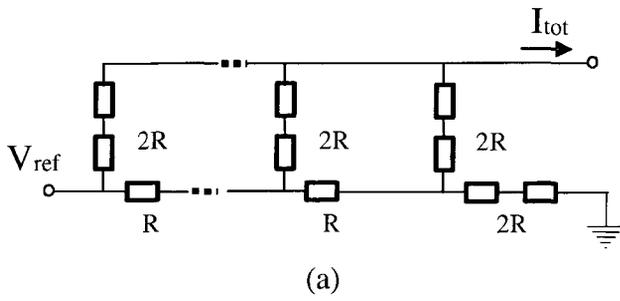


Fig.2. Area distribution of standard R-2R ladders (a) “conventional series” and (b) “conventional parallel” configurations

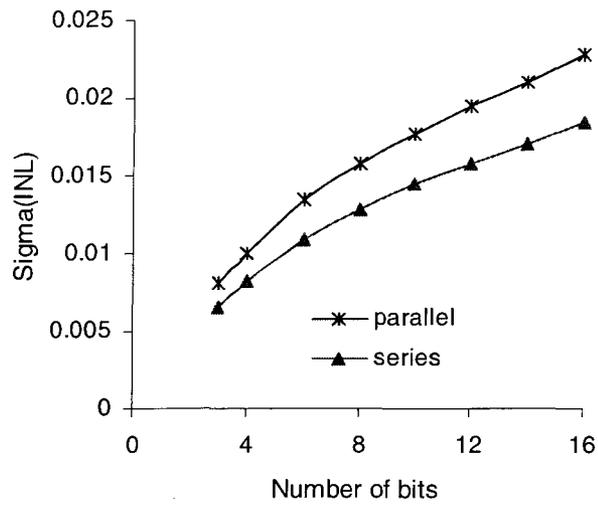


Fig.3 Sigma INL vs. resolution level

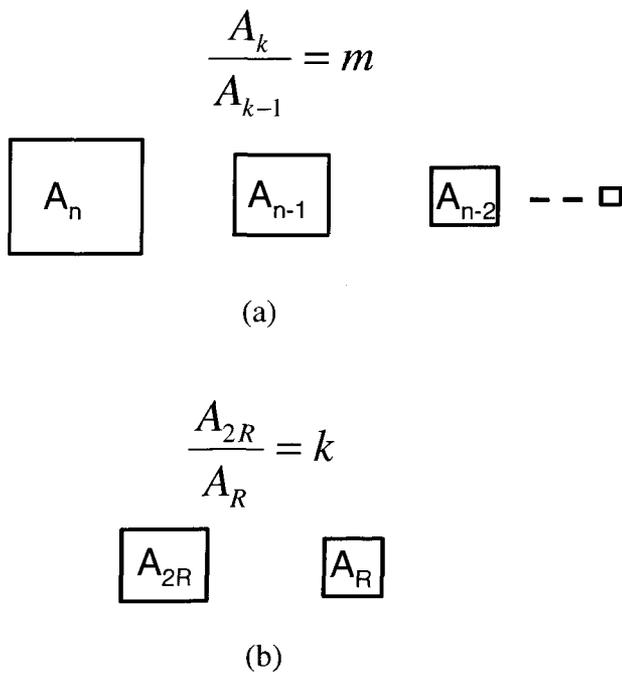


Fig.4. Area allocation of R-2R ladder cells (a) inter-slice allocation and (b) intra-slice allocation

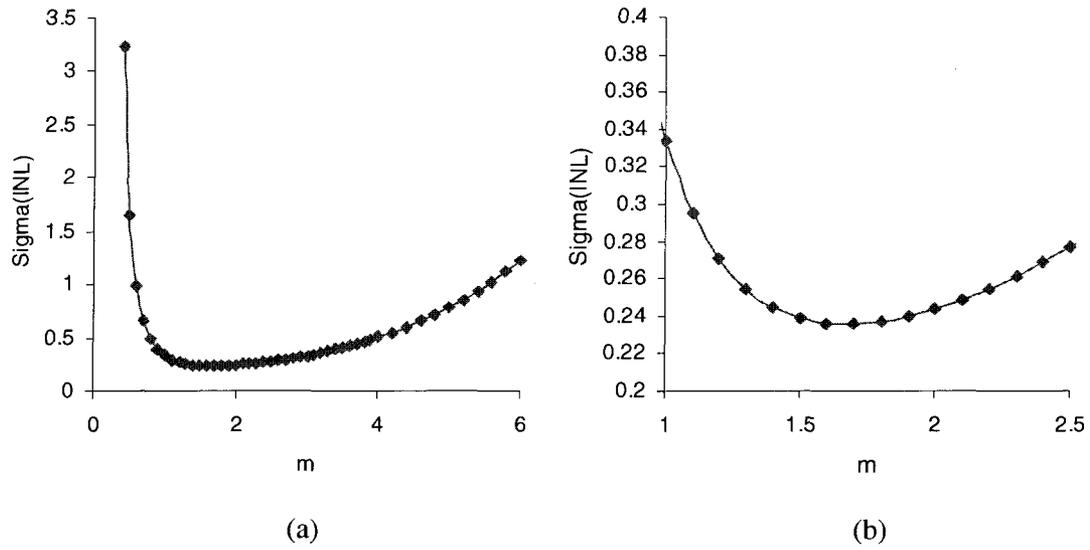


Fig.5. Standard deviation of INL vs. m for an 8-bit R-2R ladder with $k = 2$ (a) coarse view (b) expanded view

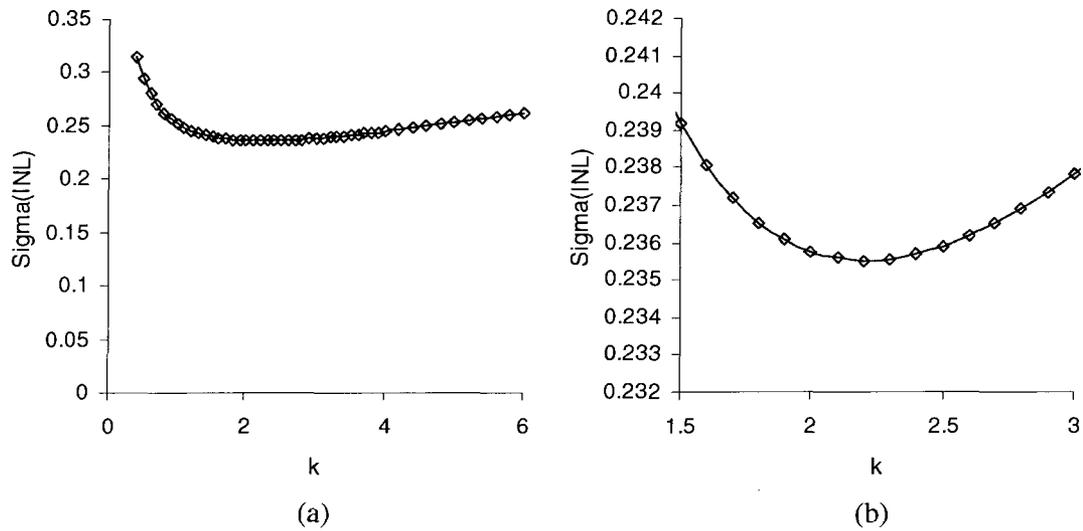


Fig.6. Standard deviation of INL vs. k for an 8-bit R-2R ladder with $m = 1.7$ (a) coarse view (b) expanded view

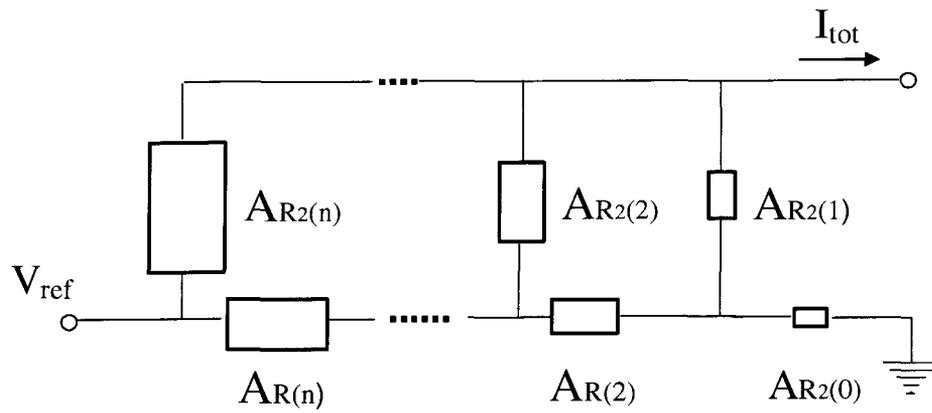


Fig.7. The area distribution of three-parameter approach

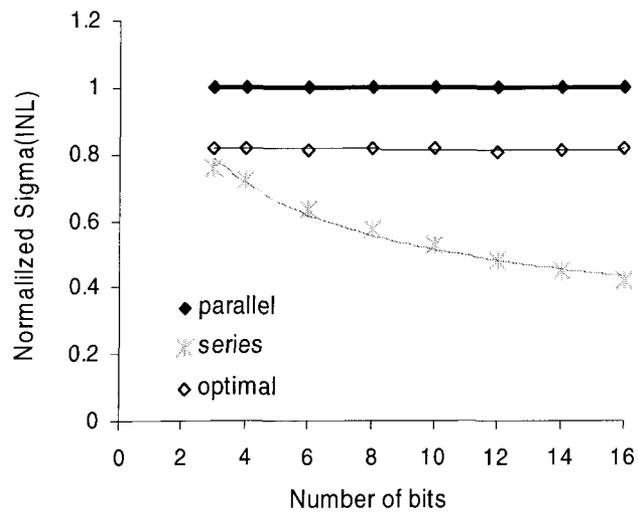


Fig.8. The normalized sigma INL of R-2R ladder vs. resolutions

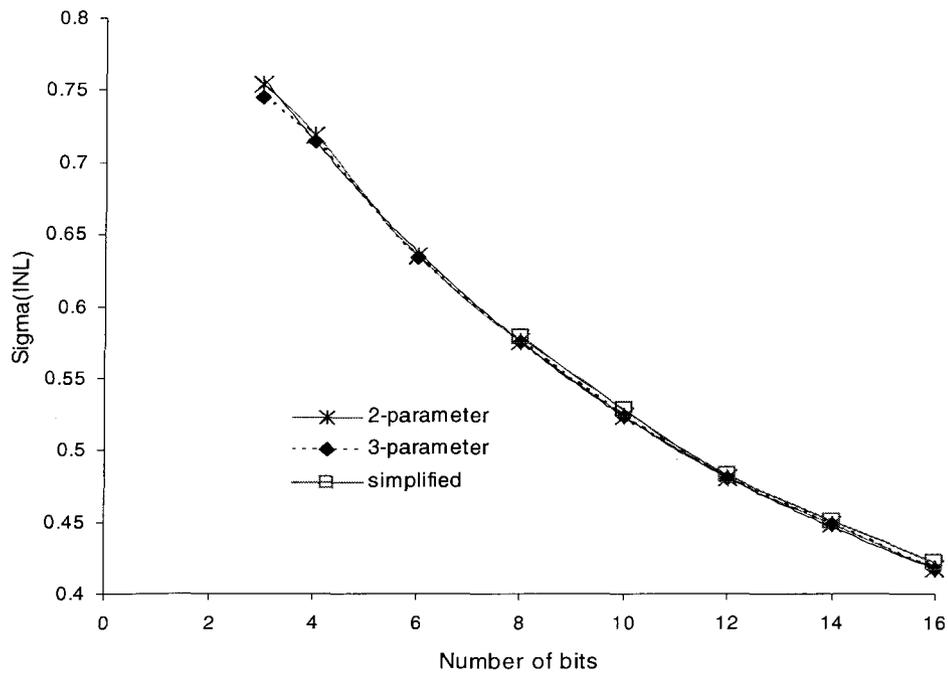


Fig.9. The normalized sigma INL of R-2R ladder vs. resolutions of three different optimal approaches

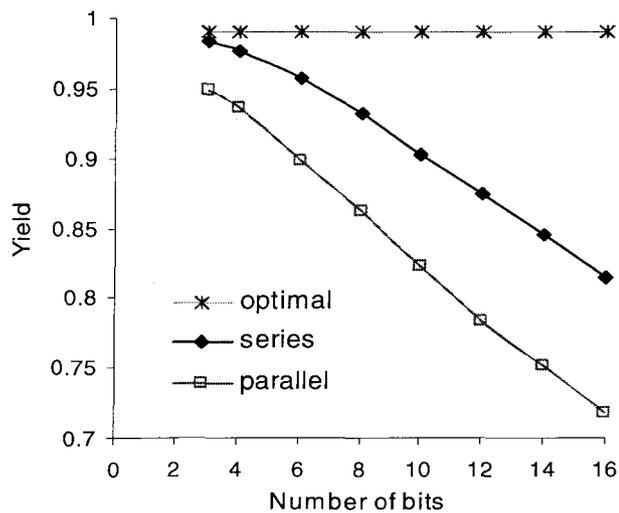


Fig.10. The yield of different area configuration of R-2R ladder vs. resolutions with same total resistor area

CHAPTER 3. YIELD ENHANCEMENT WITH OPTIMAL AREA ALLOCATION FOR RATIO-CRITICAL ANALOG CIRCUITS

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Abstract

Parametric yield models for widely used area allocation schemes in ratio-critical analog circuits are developed. It is shown that some of the most widely used schemes are suboptimal and that significant improvements in parametric yield can be achieved with less intuitive area allocation approaches. Simulations results are presented which show quantitatively what improvements in yield can be achieved with improved area allocation strategies for resistive feedback amplifiers and R-2R ladders.

I. Introduction

It is well known that different layouts of a given matching-critical circuit can have significantly different performance and yield and considerable effort is often focused on developing good layout strategies. Much of this effort has been focused on managing gradient effects, propagation delays, ohmic voltage drop in interconnects, and parasitic capacitances. Gradient-tolerant layouts including segmented common-centroid structures, path-length matching, orientation awareness, the use of dummy devices on the periphery of matching critical components, and careful sizing of interconnects have proven useful for improving effective matching performance [1-3]. Local random variations in process parameters, however, are often a significant contributor to performance degradation and

parametric yield loss and none of the layout strategies mentioned provide any relief for the problems caused by the local random variations. Unless some form of calibration is incorporated, about the only effective method most designers use for managing the adverse effects of local random parameter variations is to increase the area or physical size of the matching-critical components. It is well known that the standard deviation of many performance parameters of interest often decreases proportionally to the reciprocal of the square root of the area [1, 4-7]. Thus, a factor of 4 increase in area is required for each factor of 2 reduction in the standard deviation of the random component of the performance parameter. In addition to the adverse effect on device area, the larger devices often introduce additional parasitic capacitances and limit the speed of operation of the circuit, and in some cases also increase the power dissipation.

Invariably the area allocated to matching-critical passive and active devices is dependent upon and often proportional to the component value of the devices. For example, the area conventionally allocated by designers to each of the “R” resistors in an R-2R ladder is the same and the area allocated to each of the “2R” resistors is also the same. Correspondingly, if the ratio of two resistors is K, the area allocated to one of the two resistors is conventionally K times of the area allocated to the other resistor. This component-ratio based area allocation strategy is natural and supports the concept of realizing a ratio-critical circuit with the appropriate interconnection of unit cells.

Considering the cost of the silicon area not only in terms of the real estate but also the performance implications associated with the area-dependent parasitic capacitances and power dissipation, the question naturally arises: Is the component-ratio based area allocation strategy optimal? or, equivalently, Can parametric performance and yield be improved

within a fixed silicon area constraint with other area allocation strategies ?

In this paper, we focus on the relationship between parametric performance, parametric yield, and area allocation in matching-critical circuits. In particular, the issues of area allocation in feedback networks, R-2R ladders, and resistor string DACs are addressed.

In what follows it will be assumed that the only nonideal effects are the random variation in matching critical components. That is, the effects of gradients, placement, and orientation of matching-critical components will not be considered but it will be assumed that known existing layout strategies including segmentation, common-centroid layouts, and peripheral dummy devices are used to manage such nonideal effects. The beneficial properties, ensuring from good layout strategies that provide insensitivity to local non-random variations are, in general, not adversely affected by the optimal area allocation strategies introduced in this paper.

As an example, for a negative feedback amplifier with a nominal gain of -16, if an optimal area allocation strategy is used instead of the widely-used component-ratio area allocation approach, it will be shown that the parametric yield due to local random variations in the sheet resistance can be increased from 78% to 99% with the same total area in a typical process.

With decreasing feature sizes in emerging processes, the cross-sectional area of contacts is decreasing with feature size. This is driving up the contact resistance and usually increasing the variance of the contact resistance between two closely-placed contacts. The implication is that the effective resistance of film resistors is becoming increasingly dependent upon contact resistance and the variance of the effective resistance is becoming increasingly dependent upon the variance of the contact resistances. A statistical model for

the effects of contact resistance on the performance of matching-critical circuits is also discussed and included in the formulation of the area allocation problem in matching-critical circuits.

II. Area-Partitioning

If the gradient effects are neglected, it is well-known that the standard deviation of the normalized resistance of any rectangular resistors of length L and width W due to local random variations in the sheet resistance can be expressed as [6]:

The effects of local random variations in the sheet resistance on the resistance of a rectangular film resistor depicted in Fig.1 will be considered in this section. In this simplified description, the resistor body is a rectangular region of length L and width W with contacts along the left and right sides of the resistor. The film material that comprises the resistor body is assumed to be homogeneous, that is, the nominal sheet resistance is independent of position in the resistor body. It will be assumed initially that the contact resistance of the rectangular resistor is 0Ω . It will also be assumed that the local random variations in the sheet resistance from one point to another distinct point are uncorrelated, and that the length L and width W are equal to their nominal values. Comments about the random variations in W or L , which may play a role in matching properties when W or L is small, will be made later. With these assumptions, it follows that the nominal resistance of a rectangular resistor is given by the expression

$$R_N = R_{\square N} \frac{L}{W} \quad (1)$$

where $R_{\square N}$ is the nominal value of the sheet resistance. The variance of the normalized

resistance can be expressed as [1, App., 5, 8]

$$\sigma_{\frac{R}{R_N}}^2 = \frac{1}{WL} \cdot \left(\frac{A_\rho}{R_{\square N}} \right)^2 = \frac{1}{A_R} \cdot \left(\frac{A_\rho}{R_{\square N}} \right)^2 \quad (2)$$

where the random variable R is the resistance, A_ρ is a process parameter that characterizes the random local sheet resistance variation, and A_R is the area of the resistor.

A. Feedback Amplifiers

A basic negative feedback amplifier is shown in Fig.2. The gain, θ , of the amplifier is given by the well-known expression $\theta = -R_B/R_A$ [9] where the resistors R_A and R_B are random variables that differ from their nominal values because of the local random variations in the sheet resistance. The nominal value of the gain is given by the expression $\theta_N = -R_{BN}/R_{AN}$ where R_{AN} and R_{BN} are the nominal values of the resistors R_A and R_B respectively. The random variables $R_A - R_{AN}$ and $R_B - R_{BN}$ are assumed to be uncorrelated with zero mean and have a nearly Gaussian distribution [10, 11]. If the random component of R_A or R_B is appreciable relative to the nominal component, a closed-form explicit expression of the probability density function (PDF) of the gain is difficult or impossible to obtain. In such situations, however, the gain accuracy would be so poor that these amplifiers would be of little use in precision applications. Correspondingly, in the practical applications of interest in this work where accurate gain is required, the random component of R_A , denoted as R_{AR} , and the random component of R_B , denoted as R_{BR} , must be very small relative to the nominal component if reasonable yields are to be obtained. In these situations, it can be shown that the normalized gain can be approximated by the expression.

$$\frac{\theta}{\theta_N} \approx 1 - \frac{R_{AR}}{R_{AN}} + \frac{R_{BR}}{R_{BN}} \quad (3)$$

where θ_N is the nominal gain, i.e. $\theta_N = -\frac{R_{BN}}{R_{AN}}$.

Since R_{AR} and R_{BR} are independent Gaussian random variables and since it is well known that the linear combination of Gaussian random variables is Gaussian, it follows that the normalized gain is also Gaussian with variances given by this expression

$$\sigma_{\frac{\theta}{\theta_N}}^2 = \sigma_{\frac{R_A}{R_{AN}}}^2 + \sigma_{\frac{R_B}{R_{BN}}}^2 \quad (4)$$

It follows from (2) and (4) that the variance of the normalized gain can be rewritten as

$$\sigma_{\frac{\theta}{\theta_N}}^2 = \left(\frac{1}{A_{R_A}} + \frac{1}{A_{R_B}} \right) \cdot \left(\frac{A_\rho}{R_{\square N}} \right)^2 \quad (5)$$

where A_{R_A} and A_{R_B} are the areas of R_A and R_B respectively.

Two natural methods for area allocation for the resistors are what we term the “conventional series” allocation and the “conventional parallel” allocation. If θ_N is an integer, the conventional series allocation is characterized by the formation of R_B with the series connection of θ_N unit cells while R_A is comprised of a single unit cell. This is depicted in Fig.3a. The unit cell itself may be physically a series or parallel combination of smaller unit cells if a common centroid layout is used to minimize gradient effects. Correspondingly, the conventional parallel allocation is characterized by the formation of R_A with the parallel connection of θ_N unit cells while R_B is comprised of a single unit cell. This is depicted in Fig.3b.

If A_{CELL} is the area of the unit cell, it follows from (5) that the variance of θ_N for both of the conventional area allocation strategies is given by

$$\sigma_{\frac{\theta}{\theta_N}}^2 = \frac{1}{A_{CELL}} \cdot \left(1 + \frac{1}{\theta_N}\right) \cdot \left(\frac{A_\rho}{R_{\square N}}\right)^2 \quad (6)$$

or, if A_T is the total area allocated to the resistors, it can be expressed in terms of A_T as

$$\sigma_{\frac{\theta}{\theta_N}}^2 = \frac{1}{A_T} \cdot \left(\frac{1}{\sqrt{\theta_N}} + \sqrt{\theta_N}\right)^2 \cdot \left(\frac{A_\rho}{R_{\square N}}\right)^2 \quad (7)$$

It follows from (7) that the standard deviation of the gain can be expressed as

$$\sigma_\theta = \frac{1}{\sqrt{A_T}} \cdot (\theta_N^{0.5} + \theta_N^{1.5}) \cdot \left(\frac{A_\rho}{R_{\square N}}\right) \quad (8)$$

It should be apparent from (8) that for a fixed total area, the standard deviation increases rather rapidly with θ_N and that for large gains, it increases with $\theta_N^{1.5}$.

Both the conventional series and conventional parallel area allocation strategies can be viewed as component-ratio based area allocation schemes since the area allocated to the resistors is proportional to the values of the resistors.

The issue of optimal area allocation for a fixed total resistor area will now be addressed. It follows from (5) that the variance can be expressed in terms of A_T as

$$\sigma_{\frac{\theta}{\theta_N}}^2 = \left(\frac{1}{A_{R_B}} + \frac{1}{A_T - A_{R_B}}\right) \cdot \left(\frac{A_\rho}{R_{\square N}}\right)^2 \quad (9)$$

If this expression is minimized for a fixed A_T with respect to A_{R_B} , it follows from a simple derivation that the variance is minimized if

$$A_{R_A} = A_{R_B} = \frac{A_T}{2} \quad (10)$$

and $\sigma_{\frac{\theta_{\min}}{\theta_N}}^2$ is given by

$$\sigma_{\frac{\theta_{\min}}{\theta_N}}^2 = \frac{4}{A_T} \cdot \left(\frac{A_p}{R_{\square N}} \right)^2 \quad (11)$$

It follows from (11) that the standard deviation of the gain for the optimal area allocation can be expressed as

$$\sigma_{\theta} = \frac{2\theta_N}{\sqrt{A_T}} \cdot \left(\frac{A_p}{R_{\square N}} \right) \quad (12)$$

These results can be summarized with the layout principle for ratio-matched resistors:

Layout Principle for Ratio-Matched Resistors: The effects of local random variations in sheet resistance in the ratio matching accuracy of two rectangular resistors will be minimized for a given total resistor area if equal area is allocated to the two resistors.

A comparison of (7) with (11) shows a rather substantial difference. Specifically, the conventional series and conventional parallel allocation strategies have a standard deviation dependent upon $\theta_N^{1.5}$ whereas the optimal area allocation strategy has a standard deviation dependent upon θ_N . This difference can be quite significant for large gains.

As an example, if an amplifier with a gain of 16 is implemented with the conventional series area allocation, the standard deviation will increase by a factor of 2.125 over that for an optimal area allocation. This difference may be better appreciated from a parametric yield comparison. If the gain of 16 must be accurate to 1% and the total resistor area is allocated to achieve a 99.999% parametric yield with an optimal area allocation scheme, then the

parametric yield would drop to 96.75% for either the conventional series or the conventional parallel area allocation strategy. Although it may appear that this is only a drop of 3.25% in yield, the economical impact of this yield drop is very significant. For example, if a circuit required 32 channels with a gain of 16 all with an accuracy requirement of 1%, then the optimal area allocation strategy, assuming a Gaussian distribution, would provide a parametric yield of $.99999^{32} = 99.97\%$ whereas that of the conventional series layout would be $.9675^{32} = 34.74\%$.

In some cases it may not be convenient to exactly allocate the same area to R_A and R_B . Such might be the case, for example, if the desired gain is 3. In these cases, it is useful to quantify the parametric yield loss or correspondingly the deterioration in the standard deviation of the gain from the optimal value. If we define the area split factor γ by the expression $\gamma = \frac{A_{RB}}{A_r}$, it follows from (9) and (11) that

$$\sigma_{\theta} = \sigma_{\theta \min} \frac{1}{2\sqrt{\gamma(1-\gamma)}} \quad (13)$$

where it is apparent that the standard deviation achieved its minimum value when $\gamma = 1/2$.

A plot of the normalized standard deviation of the gain versus γ is shown in Fig.4. From this plot it is apparent that the minimum at $\gamma = 1/2$ is shallow but that the standard deviation penalty goes to infinity if the area differences are large. For example, if we want the standard deviation to be at most 0.5% above the optimal value, then $0.4502 \leq \gamma \leq 0.5498$ whereas if a 1% deviation is acceptable, then $0.4298 \leq \gamma \leq 0.5702$. A near-minimum standard deviation and correspondingly near optimal yield will be achieved only if the standard deviation of the ratio is within the insensitive shallow region of the curve in Fig.4.

An example of where it is not practical to achieve an equal split in the area but where near optimal yield is still achievable is worth mention. If the desired gain is 8, then R_B can be implemented with eight unit resistors in series and R_A can be implemented with nine unit resistors in a 3 by 3 series-parallel combination. This results in a γ value of 8/17 which is in the insensitive shallow region near the optimal value of $\gamma = 1/2$.

An appreciation for the significance of the improvement of the optimal area allocation strategy relative to that of the conventional series layout or the conventional parallel layout can be obtained from Fig.4. It should be apparent that for small gains, the benefits for going from the conventional series or the conventional area allocation strategy to the optimal area allocation strategy are minimal. However, the benefits are very significant when large gains, e.g. 100 with the series or parallel layout designated with points X_{100S} and X_{100P} in Fig.4, are required.

When large gains are required it is apparent from (11) that even with the optimal area allocation strategy, the standard deviation increases with the gain. There is also concern about the large component spread required to achieve large gains. There are two common strategies used for reducing the component spread. One uses the cascade of lower gain stages and the other is based upon using a T-feedback network. These are depicted in Fig.5a and Fig.5b respectively. The issue of what impact these alternate architectures have on gain accuracy with the presence of random variations in sheet resistance will now be investigated.

For the cascaded amplifier of Fig.5a, it can be shown following a technique similar to that used for the basic amplifier of Fig.2 that the standard deviation of the gain will be minimized if

$$A_{R_1} = A_{R_2} = A_{R_3} = A_{R_4} = \frac{A_T}{4} \quad (14)$$

and $\sigma_{\frac{\theta_{\min}}{\theta_N}}^2$ is given by

$$\sigma_{\frac{\theta_{\min}}{\theta_N}}^2 = \frac{16}{A_T} \cdot \left(\frac{A_\rho}{R_{\square N}} \right)^2 \quad (15)$$

A comparison of (11) and (15) shows that the standard deviation doubles when the same gain is realized with a cascade of two amplifier stages. This can cause a significant penalty in yield if the cascaded amplifiers are used instead of using a single stage amplifier. For a cascade of k amplifiers, it can be shown that the standard deviation will be minimized if all resistors have the same area which is $A_T / 2k$ and the corresponding minimum variance is given by

$$\sigma_{\frac{\theta_{\min}}{\theta_N}}^2 = \frac{4k^2}{A_T} \cdot \left(\frac{A_\rho}{R_{\square N}} \right)^2 \quad (16)$$

It should be apparent that the penalty in the yield for a given area becomes significant if a large number of cascaded gain stages are used.

The analysis of the amplifier with the T-feedback network is somewhat more tedious. It is straightforward to show that the magnitude of the nominal gain of the amplifier of Fig.5b is given by the expression

$$\theta_N = \frac{R_{2N}}{R_{1N}} \left(1 + \frac{R_{4N}}{R_{2N}} + \frac{R_{4N}}{R_{3N}} \right) \quad (17)$$

and the variance of the gain is given by

$$\sigma_{\theta}^2 = a_1^2 \sigma_{\frac{R_{1r}}{R_{1N}}}^2 + a_2^2 \sigma_{\frac{R_{2r}}{R_{2N}}}^2 + a_3^2 \sigma_{\frac{R_{3r}}{R_{3N}}}^2 + a_4^2 \sigma_{\frac{R_{4r}}{R_{4N}}}^2 \quad (18)$$

where the subscript ‘‘r’’ denotes the random part of the variable and the subscript ‘‘N’’ denotes the nominal part of the variable. The intermediate variables a_1, a_2, a_3 and a_4 are defined by

$$a_1 = \left| R_1 \frac{\partial \theta}{\partial R_1} \right| = \frac{R_{2N}}{R_{1N}} \left(1 + \frac{R_{4N}}{R_{2N}} + \frac{R_{4N}}{R_{3N}} \right) \quad (19)$$

$$a_2 = \left| R_2 \frac{\partial \theta}{\partial R_2} \right| = \frac{R_{2N}}{R_{1N}} \left(1 + \frac{R_{4N}}{R_{3N}} \right) \quad (20)$$

$$a_3 = \left| R_3 \frac{\partial \theta}{\partial R_3} \right| = \frac{R_{2N}}{R_{1N}} \frac{R_{4N}}{R_{3N}} \quad (21)$$

$$a_4 = \left| R_4 \frac{\partial \theta}{\partial R_4} \right| = \frac{R_{4N}}{R_{1N}} \left(1 + \frac{R_{2N}}{R_{3N}} \right) \quad (22)$$

If A_{R1}, A_{R2}, A_{R3} and A_{R4} are the areas of $R_1 \dots R_4$ respectively, it follows after substituting (2) into (18) that

$$\sigma_{\theta}^2 = \left(\frac{A_p}{R_{DN}} \right)^2 \cdot \left(\frac{a_1^2}{A_{R1}} + \frac{a_2^2}{A_{R2}} + \frac{a_3^2}{A_{R3}} + \frac{a_4^2}{A_{R4}} \right) \quad (23)$$

If A_T is the total area, we can express the constraint equation as

$$A_T = A_{R1} + A_{R2} + A_{R3} + A_{R4} \quad (24)$$

Minimizing the variance in (23) with the constraint of (24), we obtain the optimal area allocations

$$A_{Rk OPT} = \frac{a_k}{\sum_{k=1}^4 a_k} \cdot A_T \quad k = 1, 2, 3, 4 \quad (25)$$

Substituting (25) into (23) and combining with (17)-(22), $\sigma_{\theta \min}^2$ is given by

$$\sigma_{\frac{\theta_{\min}}{\theta_N}}^2 = \left(1 + \frac{1}{\frac{R_{3N}}{R_{4N}} + \frac{R_{3N}}{R_{2N}} + 1} \right)^2 \cdot \frac{4}{A_T} \cdot \left(\frac{A_p}{R_{DN}} \right)^2 \quad (26)$$

Compared to (11), $\sigma_{\frac{\theta_{\min}}{\theta_N}}^2$ for T-feedback network is always larger than that of basic structure, because here the first term in the bracket is always larger than one.

Although the closed form solution appears to be quite simple, when expressed in terms of the component values in the circuit, it becomes quite unwieldy. A numerical comparison of the T-feedback network amplifier with the basic single-stage amplifier and the cascaded structures, all under the assumption of optimal area allocation with the same total resistor area, will now be made. If the magnitude of the overall gain is to be 100, the standard deviation for the basic amplifier is given by $200 \frac{A_p}{R_{DN} \sqrt{A_T}}$, that of a two amplifier cascade is given by $400 \frac{A_p}{R_{DN} \sqrt{A_T}}$, that of a three amplifier cascade is given by $600 \frac{A_p}{R_{DN} \sqrt{A_T}}$ and that of the T-network with $R_2=R_4=10R_1$ and $R_3=1.25R_1$ is given by $360 \frac{A_p}{R_{DN} \sqrt{A_T}}$. The deterioration in the standard deviation from that attainable with the basic single-stage amplifier should be apparent.

B. R-2R DACs

The basic R-2R ladder network depicted in Fig.6, with appropriate termination resistors on the two-port, is widely used in R-2R DACs and other integrated applications because of what most view as two attractive properties. One is the linear increase in area with resolution. The other is the ability to implement the ladder with multiple instantiations

of a single unit cell with each additional bit of resolution requiring only 3 additional unit cells. Inherent in the rationale behind this view is the unquestioned premise that the area allocated for each R-2R segment is the same irrespective of the number of bits of resolution of the structure. Consistent with this view are two standard area allocation schemes for implementing the R-2R ladder. One uses two unit cells connected in series to realize each of the “2R” resistors and a single unit cell to realize each of the “R” resistors as depicted in the bit-cell of Fig.7a. This is descriptively termed the “conventional series” area allocation strategy. The second area allocation scheme uses two unit cells connected in parallel to form each of the “R” resistors and a single unit cell to realize the “2R” resistors as depicted in Fig.7b. This is descriptively termed the “conventional parallel” area allocation strategy.

There are several variant applications of the R-2R network. The question of whether the conventional series or the conventional parallel area allocation offers better performance naturally arises but once this question is raised, the more general question of whether either of these is optimal deserves consideration. It has been previously shown [12, 13] that the conventional series and the conventional parallel area allocations are not optimal in one application. It will also be shown here that the optimal area allocation strategy is application dependent.

An application of the R-2R network in an n-bit DAC that was an (n-1) stage R-2R structure is shown in Fig.8. This structure has $(2n-1)$ resistors grouped as (n-1) bit slices denoted as slice(2), ..., slice(n) in the Figure. There is one termination resistor, denoted as $R_2(T)$, has been included in the n^{th} bit slice. The DAC ideally has $N=2^n$ output levels. Since emphasis is on the performance of the R-2R network, it will be assumed that the current sources are all matched and that the op amp is ideal. The linearity of a DAC is one of the

most important characteristics of the DAC in many applications. Various metrics are used to characterize the linearity of a DAC. One of the most widely used metrics is the Integral Nonlinearity (INL), defined relative to a fit line between the end points of the transfer characteristics [14]. The INL is generally expressed relative to the ideal change in the output due to a Least Significant Bit (LSB) change in the Boolean input [14]. This output change is denoted as an LSB change in the output. The endpoint INL in LSB for output $k, 0 \leq k \leq N-1$, is given by the equation:

$$INL_k = \frac{I_k - I_0 - k \left(\frac{I_{N-1} - I_0}{N-1} \right)}{\left(\frac{I_{N-1} - I_0}{N-1} \right)} \quad (27)$$

where I_k is the current I_{OUT} corresponding to the Boolean input with decimal equivalent k . The INL is defined to be the maximum of the absolute values of the INL_k and is formally expressed as:

$$INL = \max_{0 \leq k \leq N-1} \{|INL_k|\} \quad (28)$$

The standard deviation of the INL is denoted by σ_{INL} . The INL is a random variable and is the N^{th} order statistic of the N correlated random variables, $\{|INL_k|, 0 \leq k \leq N-1\}$. Analytical expressions for statistics of the INL such as σ_{INL} are not mathematically tractable. This information is, however, essential for soft yield prediction and for determining the optimal area allocation strategy in the R-2R network. Computer simulations can be used for characterizing the INL. For this characterization it will be assumed that the total area A_T , for an n -bit R-2R ladder is fixed. The optimal area allocation problem for the $(n-1)$ stage R-2R ladder of Fig.8 is thus that of determining the area that should be allocated to each of the $(2n-$

1) resistors in the R-2R ladder so that the standard deviation of the INL, σ_{INL} , is minimized. Formally, if the variables $\{A_1, \dots, A_{2n-1}\}$ denoted the areas of the $(2n-1)$ resistors, then the optimal area allocation problem becomes that of determining $\{A_1, \dots, A_{2n-1}\}$ that will minimize σ_{INL} subject to the constraint $\sum_{i=1}^{2n-1} A_i = A_T$. This $(2n-1)$ parameter optimization problem with one constraint is not readily solvable even with a simulator when n is large because of the large number of calculations needed to determine the INL. A near optimal solution can be obtained, however, by making three simplifying assumptions that will dramatically reduce the dimensions of the optimization space. These assumptions are the following.

- 1) The ratio of the area allocated to bit slice j , denoted as A_{B_j} , to that allocated to bit slice $(j+1)$, denoted as $A_{B_{j+1}}$ is constant for all $2 \leq j \leq (n-1)$. This ratio can be characterized by the parameter m , thus

$$m = \frac{A_{B_j}}{A_{B_{j+1}}} \quad 2 \leq j \leq (n-1) \quad (29)$$

- 2) The ratio of the area allocated to the “2R” resistor, $R_2(j)$, in bit slice j , denoted as A_{2R_j} , to that of the “R” resistor, in the same bit slice, denoted as A_{R_j} , is constant for bit slice(2) to $(n-1)$. This ratio can be characterized by the parameter k , thus

$$k = \frac{A_{2R_j}}{A_{R_j}} \quad 2 \leq j \leq (n-1) \quad (30)$$

- 3) The ratio of the area allocated to the two “2R” resistors, $R_2(T)$ and $R_2(n)$,

denoted as $A_{2R(T)}$ and $A_{2R(n)}$, to that of the “R” resistors, denoted as A_{R_n} in the n^{th} bit slice is k , thus

$$k = \frac{A_{2R(T)} + A_{2R(n)}}{A_{R_n}} = \frac{2A_{2R(n)}}{A_{R_n}} \quad (31)$$

With these assumptions, the two parameters m and k uniquely determines the area allocation and reduces the size of the optimization space from $(2n-1)$ variables to 2 variables. This two-variable optimization is thus that of obtaining values of k and m that minimize σ_{INL} .

For convenience, a C-program was developed to perform this optimization using a standard statistical simulation approach. In this simulation, it was assumed that every resistor can be expressed as $R = R_N + R_R$ where R_N is the nominal value and R_R is a random component of the resistor. It was assumed that R_R is a Gaussian variable with mean of zero and standard deviation of $\sigma = \frac{A_\rho}{R_{UN} \cdot \sqrt{A_R}}$ where the A_R is the area assigned to this resistor as determined by the m and k values and A_T . It can be shown that the optimal values for m and k are not dependent on A_T , A_ρ , or R_{UN} . Thus, for convenience in the optimization, a total area A_T was selected so that a resistor with area A_T will have a standard deviation of 0.1%. For each estimate of (m, k) in the simulation, 10,000 DACs were generated by randomly selecting resistor values from the Gaussian distribution just described. For each of the 10,000 DACs, the INL was determined. The mean and standard deviation of the INLs were computed. With this two-variable optimization, optimal values of m and k were determined to be $m \approx 1.6$ and $k \approx 0.7$. Since k is somewhat less than unity, this would suggest that the conventional parallel layout should give better performance than the conventional series layout. A plot of the standard deviation in the INL versus m for fixed k and versus k for

fixed m which shows the sensitivity of the standard deviation to each of these parameters is shown in Fig.9. The plot in Fig.9b is an expanded version of that of Fig.9a. This plot shows that the local minimum is quite shallow in either the m or k variable—suggesting that near optimum performance can be obtained even if m and k differ somewhat from their optimal values but the yield penalty will be quite large if m deviates significantly from the optimum.

It is useful to make a comparison of the optimal area allocation approach with the conventional series and the conventional parallel area allocation strategies discussed above. It can be shown that the conventional series strategy is characterized by $m=1$ and $k=2$ and the conventional parallel strategy is characterized by $m=1$ and $k=0.5$. Fig.10 shows comparisons of the standard deviation of the INL, σ_{INL} , and the mean of the INL, μ_{INL} , of the optimal area allocation strategy with those of the conventional series and the conventional parallel strategies. For convenience, we have assumed a process with $\frac{A_p}{R_{DN}} = 0.1314 \mu m$. In this figure, σ_{INL} and μ_{INL} are plotted versus area for different resolution levels. Each point of the curve was obtained from a sample of 10,000 INLs generated by the same method used in the optimization. It can be observed that the conventional parallel layout has a lower standard deviation than the conventional series layout but both are appreciably larger than that of the optimal area allocation strategy. The implications on yield of these differences in standard deviation will be discussed in the next section.

The issue of optimality of the two-variable optimization instead of a $(2n-1)$ -variable optimization deserves comments. In related work [12,13], a more general three-variable optimization of a closely related optimization problem showed little difference between the two-variable and the three-variable optimization. All that we can claim here, however, is that

this two-variable optimization results in an area allocation that provides a significant improvement in performance for a given area when compared to a standard area allocation strategy. We do believe however, that two-variable optimization does provide near optimal values for m and k .

An alternative application of the R-2R ladder in a DAC is shown in Fig.11. The optimal area allocation and the performance of the optimal structure relative to that of the conventional series and the conventional parallel strategies were considered in [13]. For comparison with the R-2R application of Fig.8, the previous results will be repeated here. The parameters m and k as defined by (29) and (30) can be used to characterize the R-2R DAC in this application as well. Optimal values of $m \approx 1.7$ and $k \approx 2.2$ were obtained. Although the value of m is comparable to that for the DAC of Fig.8, the value of k differs significantly suggesting that more area should be allocated to the 2R resistors than to the R resistors in contrast to the results obtained for the circuit of Fig.8. Since k is somewhat larger than unity, these results also suggest that the conventional series layout should give better performance than the conventional parallel layout for the DAC application of Fig.11, in contrast to what was observed for the application of Fig.8. A plot of the standard deviation of INL versus m for fixed k and versus k for fixed m which shows the sensitivity of the standard deviation to each of these parameters is shown in Fig.12. This plot shows that the local minimum is quite shallow in either of the m or k variable suggesting that near optimum performance can be obtained even if m and k differ somewhat from their optimal values but the yield penalty will be quite large if m deviates significantly from the optimum. It should be noted by comparing the results in Fig.9 with those in Fig.12 that there is a significant difference in the functional form of the INL for the two DAC applications. A

yield comparison of the optimal area allocation scheme for the circuit of Fig.11 with that of the conventional series and the conventional parallel layout is shown in Fig.13. In this plot the total area for the three allocation schemes is the same and the standard deviation is normalized relative to that of the conventional parallel layout. As conjectured, in contrast to the DAC application of Fig.8, these results show that the conventional series scheme gives better performance than the conventional parallel scheme. But as for the previous structure, the optimal layout gives considerably better performance than either of the conventional schemes.

These results show that the optimal area allocation strategy for the R-2R network is application dependent. Some applications favor allocating more area to the “R” resistors whereas other favors allocating more area to the “2R” resistors. Both applications, however, show that with a fixed area constraint, it is advantageous to allocate proportionally more area to the Most Significant Bit (MSB) portion of the network than towards the LSB portion. Although the geometric decrease in the scaling of area from the MSB to the LSB gives optimal performance, there are challenges associated with continued scaling of area if the number of bits of resolution is large. It was shown in [13] that the major benefit in performance for the DAC of Fig.11 is obtained from scaling of the few MSB slices and that near optimal performance can be obtained if the latter LSB slices are all equally sized and that near optimal performance can be obtained using a small number of standard unit resistors for arbitrary gain values. The same results apply to the DAC of Fig.8.

These results can be summarized with the layout principle for the R-2R DACs considered in this section.

Layout Principle for R-2R DACs: The effects of local random variations in sheet resistance in the INL for R-2R DACs comprised of rectangular resistors will be minimized for a given total resistor area if proportionally more area is allocated to the more significant bits. But the optimal area allocation is dependent upon how the R-2R network is used. The optimal area allocation for the R-2R DAC of Fig.8 corresponds to rationing the area between successive bits by 1.6 and maintaining a ratio of the area of the “2R” resistors to the “R” resistors of 0.7. The optimal area allocation for the R-2R DAC of Fig.11 corresponds to rationing the area between successive bits by 1.7 and maintaining a ratio of the area of the “2R” resistors to the “R” resistors of 2.2.

C. Resistor-String DACs

The resistor-string is also widely used in DACs and these DACs are descriptively termed “R-String DACs” or simply “String DACs”. The standard approach of implementing a resistor string is to allocate equal area to each of the resistors in the R-string. As was the case for the finite gain amplifiers and the R-2R DACs, the question of whether the equal area allocation strategy in string DACs is optimal naturally arises.

The R-string DAC is shown in Fig.14 where the resistors all have the same nominal value. The DAC has N output levels and the endpoint INL at the k^{th} output, in LSB, is given by:

$$INL_k = \begin{cases} 0 & k = 1, N \\ N \cdot \frac{\sum_{i=1}^{k-1} R_i - \frac{k-1}{N-1} \cdot \sum_{i=1}^{N-1} R_i}{\sum_{i=1}^N R_i} & 2 \leq k \leq N-1 \end{cases} \quad (32)$$

It will be assumed that the value of each resistor can be expressed as

$$R_i = R_N + R_{ir} \quad (33)$$

where R_N is the nominal value and R_{ir} is the random deviation of resistance R_i from its nominal value. With this notation, if it is assumed that

$$\sum_{i=1}^N \frac{R_{ir}}{R_N} \ll N \quad (34)$$

(32) can be rewritten as:

$$INL_k = \sum_{i=1}^{k-1} \frac{R_{ir}}{R_N} \cdot \frac{N-k}{N-1} - \sum_{i=k}^{N-1} \frac{R_{ir}}{R_N} \cdot \frac{k-1}{N-1} \quad (35)$$

If each resistor has the same area and the random part of the resistors are all uncorrelated and identically distributed with standard deviation $\sigma_{\frac{R_r}{R_N}}$, it follows from (35) that the standard deviation of INL_k can be expressed as:

$$\sigma_{INL_k} = \sigma_{\frac{R_r}{R_N}} \cdot \sqrt{\frac{(N-k) \cdot (k-1)}{N-1}} \quad (36)$$

It follows from (2) and (36) that

$$\sigma_{INL_k} = \frac{1}{\sqrt{A_k}} \cdot \sqrt{\frac{(N-k) \cdot (k-1)}{N-1}} \cdot \left(\frac{A_p}{R_{\square N}} \right) \quad (37)$$

It is apparent from (37) that σ_{INL_k} will have a maximum value around $k = \frac{N+1}{2}$. Since

$\frac{N+1}{2}$ is not an integer, the maximum value occurs at $k = \frac{N}{2}$ or $k = \frac{N}{2} + 1$ and is given by

$$\sigma_{INL_{k_{MAX}}} = \frac{1}{\sqrt{A_k}} \cdot \sqrt{\frac{N(N-2)}{4(N-1)}} \cdot \left(\frac{A_p}{R_{\square N}} \right) \stackrel{N \text{ large}}{\cong} \frac{\sqrt{N}}{2\sqrt{A_k}} \cdot \left(\frac{A_p}{R_{\square N}} \right) \quad (38)$$

A plot of σ_{INL_k} normalized with respect to the process parameters and area (for $N=64$)

appears in Fig.15. σ_{INL_k} is symmetrical about the mid-point and the peak value increases with increasing resolution.

The plot of Fig.15 suggests that the INL is strongly dependent upon the maximum of the INL_k , and that it may be possible to reduce the standard deviation in maximum of the INL_k by increasing the area allocated to mid-range resistors in the R-string relative to that of those resistors near the ends of the string. This intuition, however, may be misleading since the simple functional form of (36) was obtained from the more complex summations in (35) under the assumption that the variances of the individual resistors were the same. Of course, the issue of how the INL relates to the INL_k is also of concern.

We will now address directly the issue of minimizing the maximum of the INL_k , or, more specifically, the issue of minimizing the INL_k at the mid-range of the R-string. It follows from (35) that the mid-range INL_k is given, for large N, by the expression

$$INL_{\frac{N}{2}} \cong \frac{1}{2} \sum_{i=1}^{\frac{N-1}{2}} \frac{R_{ir}}{R_N} - \frac{1}{2} \sum_{i=\frac{N}{2}}^{\frac{N-1}{2}} \frac{R_{ir}}{R_N} \quad (39)$$

Under the assumption that the random part of the resistor values are uncorrelated, the variance of $INL_{\frac{N}{2}}$ can be expressed as

$$\sigma_{INL_{\frac{N}{2}}}^2 = \frac{1}{4} \sum_{i=1}^{\frac{N-1}{2}} \sigma_{\frac{R_{ir}}{R_N}}^2 \quad (40)$$

It follows from (2) that this can be expressed in terms of the area allocated to the i^{th} resistor in the string, A_i , by the expression

$$\sigma_{INL_{\frac{N}{2}}}^2 = \frac{1}{4} \left(\frac{A_p}{R_{DN}} \right)^2 \sum_{i=1}^{\frac{N-1}{2}} \frac{1}{A_i} \quad (41)$$

If it is assumed that the total resistor area is fixed at A_T , we obtain the constraint equation

$$A_T = \sum_{i=1}^N A_i \quad (42)$$

The minimization of $\sigma_{INL, \frac{N}{2}}^2$ with respect to the constraint of (42) results in the solution $A_i = \frac{A_T}{N}$ for all i . This indicates the mid-range INL_k will be minimized if the area allocated to all resistors is the same. This suggests that the INL will be minimized if equal area is allocated to each resistor as well. Extensive simulations were conducted in an attempt to verify that the equal area allocation strategy also minimizes the INL. The simulation time required for minimizing the INL with respect to the area is very large even for modest values of N so lower-dimensional parameterized optimizations were explored in which proportionally more as well as proportionally less area was allocated to resistors near the middle of the string. In all cases these parameterized optimizations resulted in a larger INL than what was obtained for equal area allocation. It is thus conjectured that the INL is minimized when equal area is allocated to each resistor in the R-string.

These results can be summarized with the layout principle for R-strings.

Layout Principle for Resistor Strings: The effects of local random variations in sheet resistance in the INL for Resistor String DACs comprised of rectangular resistors will be minimized for a given total resistor area if equal area is allocated to each of the resistors.

III. Contact Resistance Issue

The previous discussions were based upon the explicit assumption that the dominant contributor to mismatch is the random variations in the sheet resistance. In particular, the

effects of random variations in contact resistance and edge variations of the resistor body were neglected. In this section, the effects of random variations in contact resistance will be considered and the effects of edge variations of the resistor body will be discussed.

With the feature sizes of the process decreasing, the sizes of the contacts are also decreasing and correspondingly the contact resistance is increasing, as is the variance of the contact resistance. Unfortunately, the statistical variation of the contact resistance from one contact to the next is quite large. The effects of the random effects of the contact resistance and the combined effects of the random effects of the contact resistance and the sheet resistance will be considered in this section. It will be assumed that the contact resistance can be modeled as the sum of a nominal component and a random component where the nominal component is assumed to be the same for all contacts in a matching critical region. It will be further assumed that the random components are uncorrelated from one contact to the next. This latter assumption, which is essentially equivalent to neglecting gradient effects, will not significantly affect the results that will be developed in this section.

Fig.16 shows a symbolic layout of a rectangular resistor. In the figure, W and L are the width and length of the film resistor and t is the pitch of the contacts. If W is large enough, the number of contacts, n, is approximately given by the expression

$$n = \frac{W}{t} \quad (43)$$

A tedious but straightforward analysis (see App.) provides a good approximation of the variance of a reference resistor which includes the effects of both the random variations in the sheet resistance and the random variations in the contact resistance:

$$\sigma_{\frac{R_{UR}}{R_{UN}}}^2 \approx \left(\frac{2R_{CN}^2}{n^3 \left(\frac{2R_{CN}}{n} + R_{SHN} \right)^2} \right) \cdot \sigma_{\frac{R_{CR}}{R_{CN}}}^2 + \left(\frac{R_{SHN}^2}{\left(\frac{2R_{CN}}{n} + R_{SHN} \right)^2} \right) \cdot \sigma_{\frac{R_{SHR}}{R_{SHN}}}^2 \quad (44)$$

In this expression, R_{UN} is the nominal resistance value of unit resistor cell, R_{UR} is the random component of the cell resistance, R_{CN} is the nominal value of the resistance of a single contact, R_{CR} is the random component of a single contact resistance, R_{SHN} is the nominal value of resistance of the sheet resistor film, and R_{SHR} is the random component of the sheet resistance. The term $\sigma_{\frac{R_{CR}}{R_{CN}}}^2$ is the variance of the local random component of the contact resistance and is a constant characteristic of the process.

The first term on the right hand side of (44) is the contribution from the variance of the contact resistance and the second term is the contribution from the variation of the sheet resistance.

A standard cell is widely used in matching critical applications so that gradient effects can be cancelled by connecting an appropriate number of these standard cells in an appropriate series or parallel way to form a common-centroid layout. Although this approach will increase the total area and increase the effects of edge variations, it is usually justifiable because of the importance of minimizing gradient effects. If the resistor layout of Fig.16 is used as a unit cell, this cell has an area A_{RU} . If k of these resistors are placed in parallel or if k of these resistors are placed in series and it is assumed that the local random variations of both the sheet resistance and contact resistances are uncorrelated, it can be shown that the normalized standard deviation of the parallel or series combination is

$$\sigma_{\frac{R_{kR}}{R_{kN}}} = \frac{1}{\sqrt{k}} \sigma_{\frac{R_{UR}}{R_{UN}}} \quad (45)$$

where R_{kR} is the random part of the parallel or series combination, R_{kN} is the nominal resistance of the parallel or series combination.

Equation (45) was developed under the assumption that the local random variations of the sheet resistance and contact resistance are uncorrelated, and in this case the relationship between $\frac{\sigma_{R_{UR}}^2}{R_{UN}}$ is given by (44). However, it can be shown that (45) is applicable even if random edge variations are included or if correlations exist between the sheet resistance and the contact resistance, provided the random variations in the resistance of the unit cells are uncorrelated. The area of the parallel or series combination relates to the area of the unit cell by the relationship

$$A_{kRU} = k \cdot A_{RU} \quad (46)$$

Substituting (46) into (45), we obtain the expression

$$\sigma_{\frac{R_{kR}}{R_k}} = \frac{1}{\sqrt{A_{kRU}}} \cdot \left(\sqrt{A_{RU}} \cdot \sigma_{\frac{R_{UR}}{R_{UN}}} \right) \quad (47)$$

The first factor on the right hand side of (47) is the reciprocal of the square root of the area of the unit cell and the term in brackets is a constant characteristic of the process. This same expression holds for a parallel series array of unit cells as well. All resistances in this expression include the combined effects of the sheet resistances and the contact resistances. A comparison of (47) with (2) indicates they are of the same functional form. Specifically the normalized standard deviation of an array of parallel or series or parallel-series connected unit cells is equal to the reciprocal of the square root of the total area multiplied by a parameter that is characteristic of the process alone. All of the derivations in the previous sections for the amplifiers, the R-2R networks, and the R-string DACs were dependent only

upon the functional relationship of (2), specifically the fact that the normalized standard deviation of a component is proportional to the reciprocal of the square root of the area times a process dependent constant. Thus, all of the results of the previous section are directly applicable to unit cells that contain the local random effects of both the contact resistance and the sheet resistance. This relationship was developed under the assumption that the resistor is rectangular with a nominally homogenous sheet resistance and thus nominally uniform current density. Thus, the layout principle for ratio-matched resistors can be restated to include the effects of the random variations of the contact resistance and the effects of edge variations as:

Layout Principle for Ratio-Matched Resistors (Including Contact Resistance Effects):

The combined effects of local random variations in sheet resistance, contact resistance and edge variations in the ratio matching accuracy of two resistors will be minimized for a given total resistor area if an equal number of unit cells, connected in a parallel, series, or parallel-series configuration, are allocated to the two resistors.

By a parallel, series, or parallel series configuration of cells to form a resistor, we mean a connection where the nominal current is the same in each unit cell of the resistor. Fig.17 shows acceptable and unacceptable parallel, series and parallel/series connections.

Equation (47) does not provide an explicit relationship for the variance in terms of process parameters. The effects of edge variations on the unit cell will be negligible if L and W are large. Drennan [15] suggests, at least in some processes, the effects of width variations are negligible even if L is small. A parametric expression for $\sigma_{\frac{R_{UR}}{R_{UN}}}$ showing the effects of edged variations on the unit cell, if of concern for a given process, can be readily derived

following the approach of Pelgrom [6] or Drennan [15].

We will now concentrate on an explicit expression for the variance of the unit cell in terms of the sheet resistance and contact resistance process parameters. This can be obtained by substituting (1), (2) and (43) into (44) to obtain the relationship

$$\sigma_{\frac{R_{UR}}{R_{UN}}}^2 = \frac{1}{WL} \cdot \left(\frac{2 \cdot R_{CN}^2 \cdot \sigma_{\frac{R_{CR}}{R_{CN}}}^2 \cdot t^3 \cdot L + L^2 \cdot A_p^2}{(2R_{CN} \cdot t + R_{DN} \cdot L)^2} \right) \quad (48)$$

where W and L are dimensions of the unit cell as depicted in Fig.16. Finally, by substituting (47) into (48), we obtain an expression for the variance of a resistor of value R that is formed by a series, parallel, or series-parallel connection of k unit cells.

$$\sigma_{\frac{R}{R_N}}^2 = \frac{1}{A_{kRU}} \cdot \left(\frac{A_{RU}}{WL} \right) \cdot \left(\frac{2 \cdot R_{CN}^2 \cdot \sigma_{\frac{R_{CR}}{R_{CN}}}^2 \cdot t^3 \cdot L + L^2 \cdot A_p^2}{(2R_{CN} \cdot t + R_{DN} \cdot L)^2} \right) \quad (49)$$

Note the term in parenthesis in (49) differs slightly from unity since the effective length and the drawn length differ because of the presence of the rows of contacts on each end of the resistor as shown in Fig.16.

It is not apparent from (48) whether the random variations in the sheet resistance or the random variations in the contact resistance are dominant. For small unit cells, the contact resistance and the contact resistance variations will dominate whereas for larger cells the sheet resistance and the sheet resistance variations will dominate. We will now determine the physical characteristics of the cell that represents a transition from contact resistance variance dominated to sheet resistance variance dominated. To determine this, it can be observed from (48) that the leftmost summand in the numerator is the contribution of the contact resistance variation and the rightmost summand is the contribution of the sheet

resistance contribution. Crossover between contact resistance dominated and sheet resistance dominated will occur when these two terms are equal. Equating these terms we find that the width plays no role (provided W is wide enough that the assumption of (43) is valid) in the crossover and obtain the critical length as:

$$L_{crit} = \frac{2 \cdot R_{CN}^2 \cdot \sigma_{\frac{R_{CR}}{R_{CN}}}^2 \cdot t^3}{A_p^2} \quad (50)$$

If we assume the pitch of the contact is 4λ , (50) can be rewritten as

$$L_{crit} = \frac{2^7 \cdot \lambda^3 \cdot R_{CN}^2 \cdot \sigma_{\frac{R_{CR}}{R_{CN}}}^2}{A_p^2} \quad (51)$$

As can be seen from (51), the critical length is a process parameter. When the length of the resistor is larger than L_{crit} , the variation of sheet resistance will dominate the contribution to the variance and when smaller, the contact resistance variations will dominate.

Good statistical information about a process is essential for predicting parametric yield. Test structures that can be used to measure parameters such as A_p and $\sigma_{\frac{R_{CR}}{R_{CN}}}^2$ are necessary for process characterization. Since these parameters characterize local process variations and not gradient effects or process variations from die to die, from wafer to wafer, or from process lot to process lot, different test structures are needed to extract these parameters. Some results [16] relating to extracting these parameters have been reported in the literature but it is the author's experience that this information is often missing from a description of the technology provided by many foundries. It is also the author's experience that those responsible for extracting this information at several major semiconductor

companies either do not have test structures that are needed to extract this information or do not distinguish between the effects of local and global mismatch. The issue of propriety further limits the availability of this information in the open literature. On smaller unit cells, however, the contact resistance variations significantly dominate those of the sheet resistance variations as governed by (51).

IV. Yield Analysis

Parametric yield predictions are strongly dependent upon the statistical distributions of the random variables affecting yield. In this work, the amplifiers discussed in section II have a gain that has a random component with a nearly Gaussian distribution. In contrast, the INL of the n -bit R-2R DAC is an N th order statistics of N non-Gaussian correlated random variables where $N \approx 2n$. In the former case, closed form expression relating yield to the standard deviation of the Gaussian variables can be readily derived. Closed form expression for the yield of the R-2R DAC is not mathematically manageable. In this section we will derive expression for the yield of the amplifier structures. Graphical results will be presented to compare yield potential of the R-2R DACs.

A. Yield of Feedback Amplifier Structures

The statistical analysis in the preceding sections is used primarily to predict yield of the feedback amplifier structures. In this section, the benefits of optimal area allocation will be discussed. It is well known that if x is a performance parameter of interest and if $\Delta\mu$ defines the yield tolerance window on the parameter x about a specified value of μ , then the parametric yield with respect to random variations in the parameter x can be expressed as

$$Y = \int_{\mu-\Delta\mu}^{\mu+\Delta\mu} f(x)dx \quad (52)$$

where $f(\mathbf{x})$ is the probability density function (PDF) of \mathbf{x} .

The local random variations of parameters such as the sheet resistance and the contact resistance can be approximated with a zero-mean Gaussian distribution provided that the total parameter variation is somewhat smaller than the nominal value of the parameter. With this approximation, it is convenient to express the yield, Y , in terms of the normalized random variable $\tilde{x} = \frac{x-\mu}{\sigma}$ where σ is the standard deviation as

$$Y = \int_{-\frac{\Delta\mu}{\sigma}}^{\frac{\Delta\mu}{\sigma}} f_n(\tilde{x})d\tilde{x} \quad (53)$$

where $f_n(\tilde{x})$ is the PDF of the zero-mean unit-variance normal distribution generally designated with the distribution notation $N(0,1)$. In terms of the normalized Gaussian Cumulative Probability Density Function (CDF) $F_n(x)$, it follows from (53) that

$$Y = 2 \cdot F_n\left(\frac{\Delta\mu}{\sigma}\right) - 1 \quad (54)$$

The yield of the ratio-based area allocation strategy for the basic amplifier of Fig.2 is compared with that of the optimal area allocation strategy in Fig.18 for different closed-loop gains. In the yield comparison, it has been assumed that a good amplifier must have a gain specification that is within 1% of the target value. Since the conventional series and the conventional parallel area allocations give the same yield, a distinction between these two strategies is not necessary. In this comparison, the total area for the resistors was the same and the total area was set at the level needed to obtain a 99% yield with the optimal area

allocation. Although one might argue that even for the gain of 100, the yield drop is only a factor of approximately 2, the impact of this yield drop is most significant. For example, if an integrated circuit had an array of 100 gain of 5 amplifiers with total area allocated to obtain a yield of 99% for each of the amplifiers with optimal area allocation, the amplifier parametric yield would be $Y_{OPT} = (0.99)^5 = 95\%$ whereas if the same total area were allocated to the conventional ratio-based allocation scheme, the yield would drop to $Y = (0.39)^5 = 0.9\%$. The importance of doing a statistical analysis when making an area allocation should be apparent from this simple example. Of equally importance is the realization that significant yield penalties or equivalently area increases will be incurred if conventional area allocation strategies are used when the gain of the amplifier is large.

A comparison of the ratio-based area allocation scheme for the cascaded amplifiers and the T-feedback amplifier is made with that of the optimal area allocation scheme in Fig.19. In these comparisons, the total area was the same for each architecture and the area was allocated to obtain a 99% yield with the basic single-stage amplifier optimal area allocation. Fig.19 also shows a comparison of the yield for the conventional architecture with that of the cascaded amplifiers and that of the T-feedback amplifier. A series layout with $R_1 = R_3$ and $R_2 = R_4$ was assumed for the T-feedback amplifier. Included in this figure are the yields that would be obtained if the conventional ratio-based area allocations were used. The impact of both architecture and area allocation on yield should be apparent from this figure.

B. Yield of R-2R DACs

The yield of the R-2R ladder DAC of Fig.8 for the conventional series and the conventional parallel area allocations are compared with that of the optimal area allocation of

$m=1.6$ and $k=0.7$ in Fig.20 for varying levels of resolution. In this comparison, it has been assumed that a good R-2R DAC must have an INL less than 0.5 LSB. A similar comparison [13] for the ladder of Fig.11 with optimal values of $m=1.7$ and $k=2.2$ is shown in Fig.21. It should be apparent from Fig.21 and Fig.20 that significant improvements in yield can be obtained if an optimal area allocation strategy is used. Finally, Fig.22 shows a comparison of the yield of the two R-2R networks. In this figure, the networks are compared using the conventional series, the conventional parallel and the optimal area allocation layouts for different levels of resolution. This comparison shows that the relative yield is bit-level and area dependent. When the resolution is high, the yield improvement is more significant. It was also shown that the optimal area allocation for the R-2R DAC of Fig.8 offers higher yield than the optimal area allocation for the structure of Fig.11. The smooth curve of the yield and area relationship is intuitively expected. If a resistor has area A_1 or A_3 with A_3 larger than A_1 , then it will have smaller standard deviation of resistance with A_3 than that with A_1 . If a resistor has area of A_2 whose value is between A_1 and A_3 , then the standard deviation of resistance is also in between.

It should be observed that in the yield comparisons, the issue of the relative role of the variations in sheet resistance and in contact resistance was intentionally not raised nor was the issue of the values for the parameters that characterize the local mismatch effects. The yield comparisons were intentionally all made in the relative sense so that the results apply in the general case since the values of the process parameters have been normalized out. Although not explicitly stated, it has been assumed in the yield assessment that a unit cell was used to form all resistors and that larger resistors were obtained with series/parallel connections of the unit cell.

V. Effects of Optimal Area Allocation on Other Circuits Properties

The issue of what effect optimal area allocation has on other circuit characteristics deserves consideration. Since optimal area allocation results were all dependent only upon how area is distributed between various components and not upon the component values themselves, the designer has the option of keeping all resistance values the same as in the original circuit or scaling the resistance values when adopting an optimal area allocation approach. If the designer chooses to leave the impedance values unchanged, then the circuit schematic remains unchanged and essentially all other circuit characteristics will remain unchanged as well, except possibly for some second-order effects due to a change in parasitic in the optimal area approach. If the designer chooses to also scale the impedance values, however, when using the optimal area allocation approach, the resultant circuit schematic will change and this change could affect other characteristics of a circuit such as linearity, power dissipation, signal swing, etc.

VI. Practical Layout Considerations

The Layout Principles for area allocation that optimizes parametric yield for ratio-matched resistors and for R-2R networks give little guidance on how the layout should be done to achieve optimal performance and in many applications, it will be difficult to practically allocate area to achieve optimal yield. It should be re-emphasized that a common centroid layout is generally necessary to minimize the effects of linear gradient effects, that an interconnection of unit cells should be used to minimize the effects of length and width variations as well as contact resistance variations, and that well-known layout matching

methods such as maintaining a common cell orientation, maintaining appropriate interconnect matching, and managing peripheral or dummy peripheral devices are important. Fortunately, it was also shown that the standard deviation of the performance metrics discussed above have a rather shallow minimum and, as such, near optimal performance can be obtained even if the optimal area allocation is not precisely achieved.

The layout of the feedback resistors for an amplifier with an integer gain such as 4 or 16 is easy to achieve with optimal area allocation. For example, the gain of 4 can be achieved using two unit cells connected in series for one resistor and two unit cells connected in parallel for the second resistor and a common centroid layout of these 4 cells is straightforward. It is difficult to achieve equal area ratios, however, with some other gain values. For example, an exact area ratio of 1 with a gain of 5 or 10 can not be readily achieved but for the gain of 5, five unit cells can be connected in series to form one resistor and the parallel combination of two strings of two resistors can be used to form the second resistor. This will result in an area ratio of 1.25 or a value of $\gamma = 0.444$ which provides near optimal performance as can be seen from Fig.4. A gain of 10 can be achieved by connecting 10 unit cells in series to form one resistor and by connecting three strings of three resistors in series to form the second resistor to achieve a value of $\gamma = 0.47$.

A layout of the R-2R network to achieve the precise area allocation for minimizing the standard deviation of the INL with an interconnection of a practical number of unit cells can not be realized. As with the ratio matching problem, however, near optimal performance can be obtained with practical unit cell based common centroid layouts. In the R-2R network, the biggest benefits are obtained by maintaining slice area ratios close to the optimum on the first few most significant bits in the network with little additional benefits

derived from optimal area scaling for the latter bits in the network. As an example, consider the R-2R network of Fig. 11 with the optimal values of $m=1.7$ and $k=2.2$. If area were assigned to an 8-bit R-2R array to achieve a yield with optimal area allocation of 97.4%, simulation results show that the yield for the standard series connection with the same total area would be 66.3% and the standard parallel connection with the same total area would provide a yield of 80.1%. If the “2R” resistor in the MSB block is realized with a parallel series connection of 18 unit cells (parallel connection of 3 strings of 6 resistors), the “R” resistor in the MSB block is realized with a parallel series connection of 9 unit cells (parallel connection of 3 strings of 3 resistors), the “2R” resistor in the second MSB block is realized with a parallel series combination of 8 unit cells and the “R” resistors in the second MSB block is realized with a parallel series connection of 4 unit cells, all remaining “2R” resistors are realized with the series combination of 2 unit cells, and all remaining “R” resistors are realized with a single unit cell, simulation results show the yield will be 95.1%. Although not quite at the optimal value of 97.4%, near optimal yield is achieved with a unit cell approach that is practical and that can be laid out in a common-centroid configuration. For notational convenience we term this the $\langle 18,9,8,4,2,1,2,1,2,1,2,1,2,2 \rangle$ standard cell allocation strategy. If instead of scaling just the two MSBs, the first three MSBs are scaled with a parallel series connection using the $\langle 32,16,18,9,8,4,2,1,2,1,2,1,2,2 \rangle$ standard cell allocation strategy, simulation results show that the yield will be increased to 96.7%.

VII. Extensions

The concepts of optimal area allocation for ratio-sensitive resistor networks can be extended to ratio-sensitive transistor or capacitor structures but with some restrictions. Such

extensions will be briefly discussed in this section.

A feedback amplifier using MOS transistors biased in the triode region to form the feedback network is shown in Fig.23. The nominal gain of the amplifier is given by the expression:

$$A_G = \frac{R_{FETB}}{R_{FETA}} \quad (55)$$

where R_{FETA} and R_{FETB} are the triode-region impedances of M_A and M_B respectively. These impedances are approximately given by the expression

$$R_{FET} = \frac{L}{(V_{GS} - V_T) \cdot \mu \cdot C_{OX} \cdot W} \quad (56)$$

where W and L are the width and length of the transistor, V_T is the threshold voltage, $V_{GS} - V_T$ is the excess bias voltage of the transistor, μ is the mobility, and C_{OX} is the oxide capacitance density. If the random variation of the edges of the channel is neglected, the local random deviations of V_T , μ and C_{OX} have a standard deviation proportional to the square root of the channel area given by the expressions [4]:

$$\sigma_{\frac{\mu}{\mu_N}} = \frac{A_{\mu}}{\sqrt{A}} \quad (57)$$

$$\sigma_{\frac{V_T}{V_{TN}}} = \frac{A_{V_T}}{\sqrt{A}} \quad (58)$$

$$\sigma_{\frac{C_{OX}}{C_{OXN}}} = \frac{A_{C_{OX}}}{\sqrt{A}} \quad (59)$$

where the subscript "N" means nominal value, the parameters A_{μ} , A_{V_T} and $A_{C_{OX}}$ are process parameters characterizing the standard deviation of μ , V_T , and C_{OX} and A is the area of the channel area of the transistor. If these two transistors are biased with the same excess bias voltages, it follows from a straightforward derivation that the normalized standard deviation

of the gain can be expressed as:

$$\sigma_{\frac{A_G}{A_{GN}}} = \sqrt{\left(A_{\mu}^2 + A_{C_{ox}}^2 + \frac{V_{TN}^2 A_{V_T}^2}{(V_{GSN} - V_{TN})^2} \right) \cdot \left(\frac{1}{A_A} + \frac{1}{A_B} \right)} \quad (60)$$

where A_A and A_B are the channel areas for transistors M_A and M_B respectively and where $V_{GSN}-V_{TN}$ is the nominal excess bias voltage. If the total channel area of M_A and M_B is fixed, it follows that the standard deviation will be minimized when the area of transistors area equal. This is the same result that was obtained for the layout of resistors. As with the resistors, a unit transistor cell would be used and parallel and series interconnections of these cells would be used to realize the elements of the feedback network.

A basic current mirror is shown in Fig.24. The nominal current mirror gain is given by the expression

$$A_{MN} = \frac{W_B L_A}{W_A L_B} \quad (61)$$

If again the random variations of the edges of the channel are neglected, it can be shown that the normalized standard deviation of the mirror gain is given by the expression

$$\sigma_{\frac{A_M}{A_{MN}}} = \sqrt{\left(A_{\mu}^2 + A_{C_{ox}}^2 + \frac{4V_{TN}^2 A_{V_T}^2}{(V_{GSN} - V_{TN})^2} \right) \cdot \left(\frac{1}{A_A} + \frac{1}{A_B} \right)} \quad (62)$$

This right hand side of (62) is similar to that of (60) and thus it can be concluded that the standard deviation of the mirror gain will be minimized for a given total channel area if the channel area of the input and output devices of the mirrors are the same.

The issues of variance and absolute accuracy are distinct and a particular layout or area allocation strategy that minimizes standard deviation may not necessarily give the best overall accuracy. For example, three circuits that provide a nominal current mirror gain of 4

are shown in Fig.25. In all cases, multiple instantiations of a unit transistor cell are used to form the input and output devices. The circuit of Fig.25a is the most common and all devices have essentially the same gate and source voltages. The circuit of Fig.25b is an equal area allocation strategy and will provide the smallest variance in the mirror gain. The source voltage of the upper cell on the input is, however, different than that of the other 3 cells. The source voltages for the three upper cells on the input side in the circuit of Fig.25c are all different and different from those of the other two cells. The systematic error in the mirror gains may not be the same for the different area allocation schemes but the equal area allocation scheme will exhibit the smallest standard deviation.

Accurately controlling capacitor ratios is also of concern as is the parametric yield for analog circuits that depend upon accurate capacitor ratios. In contrast to a resistor in which the area and resistor value of a rectangular device can be independently established, a rectangular capacitor (or actually any arbitrarily shaped parallel plate capacitor) has a capacitance value that is uniquely determined by and proportional to the capacitor area. As a result, the component-ratio based area allocation scheme in which the area is allocated in proportion to the capacitor ratio is almost exclusively used for the layout of ratio-matched capacitors irrespective of whether the capacitor is a standard planar vertical structure or a thick-metal MEM device. If the parameter $\theta = \frac{C_1}{C_2}$ defines the ratio of two capacitors, the component-ratio area allocation requirement establishes a constraint in the relationship between the area of the capacitors and the total area given by

$$A_{C1} = \left(\frac{\theta_N}{1 + \theta_N} \right) A_T \quad (63)$$

$$A_{C2} = \left(\frac{1}{1 + \theta_N} \right) A_T$$

where θ_N is the nominal capacitor ratio and A_T is the total area. In what follows the discussion will be restricted to the vertical planar capacitor although similar results apply to lateral MEM structures as well. If it is assumed that the local random variations in the capacitance density are due to variations in the oxide thickness, it follows that the standard deviation of the ratio is given by

$$\sigma_\theta = \frac{A_C}{\sqrt{A_T}} \cdot (1 + \theta_N) \sqrt{\theta_N} \quad (64)$$

where A_C is a constant dependent upon the process that characterizes the local random variations in the capacitance density. This equation is similar to that of (7) for the gain of an amplifier with resistive feedback and thus it can be concluded that the yield penalty will be quite significant if capacitor ratios significantly different than 1 are required as was shown in Fig.4.

As was the case for the resistor ratios, the standard deviation for the capacitor ratio can be expressed in terms of the area of capacitor C_1 , A_{C1} , as

$$\sigma_\theta = \theta_N A_C \cdot \sqrt{\frac{1}{A_{C1}} + \frac{1}{A_T - A_{C1}}} \quad (65)$$

If the component-ratio constraint of (63) could be removed, then (65) could be minimized with respect to A_{C1} to obtain the area allocation strategy for minimizing the standard deviation which is

$$A_{C1} = A_{C2} = \frac{A_T}{2} \quad (66)$$

Paralleling the results for the ratio matching of resistors, it follows on substituting (66) into (65) that the minimum standard deviation is given by

$$\sigma_{\theta_{\min}} = 2\theta_N \frac{A_C}{\sqrt{A_T}} \quad (67)$$

Comparing with (64) it follows that for large or small values of θ_N , the minimum given by (67) is considerably lower than that obtained for the component-ratio area allocation scheme.

If ideal capacitors are available, an equal area allocation scheme or a nearly equal area allocation scheme can be used. For example, the circuit of Fig.26 shows a standard area allocation scheme and an optimal area allocation scheme for a 4:1 capacitor ratio. Whether the optimal area allocation scheme is practical or even feasible does, however, depend on applications. In many applications the floating capacitor node would cause unacceptable parasitic and/or charge accumulation that would either be unacceptable or that could possibly cause device failure.

VIII. Conclusions

Area-allocation between components in matching-critical applications has received minimal attention in the literature. Optimal area allocation strategies for several practical applications including finite gain amplifiers, R-2R networks, R-string DACs, and current mirrors have been introduced. It has been shown that the optimal area allocation strategies can provide a significant reduction in variance for a fixed total area in some useful applications and thus a significant increase in yield when compared to more standard area allocation schemes that are based upon the component ratios. It was also shown that the

random component of the contact resistance is of growing concern in applications requiring ratio-matched resistors and strategies for minimizing the variance due to contact resistances were also developed.

Appendix

A. Contact Resistance Modeling

Consider the rectangular resistor with (n) contacts on each side shown in Fig.16. If the resistance in the metal is neglected, the total resistance of this resistor can be approximated by the expression

$$R \approx \frac{1}{\sum_{k=1}^n \frac{1}{R_{C1k}}} + R_{SH} + \frac{1}{\sum_{k=1}^n \frac{1}{R_{C2k}}} \quad (\text{A1})$$

where R_{SH} is the resistance contributed by the thin film sheet resistance, R_{C1k} is the resistance of the k^{th} contact on the left hand side of the structure, and R_{C2k} is the resistance of the k^{th} contact on the right hand side of the structure.

Neglecting any gradient effects in the sheet resistance and the contact resistances, resistors R_{SH} , R_{C1k} and R_{C2k} can be expressed as

$$R_{SH} = R_{SHN} + R_{SHR} \quad (\text{A2})$$

$$R_{C1k} = R_{CN} + R_{C1kR} \quad k=1, \dots, n \quad (\text{A3})$$

$$R_{C2k} = R_{CN} + R_{C2kR} \quad k=1, \dots, n \quad (\text{A4})$$

where R_{SHN} is the nominal resistance contribution from the thin film sheet resistance, R_{SHR} is the random component of R_{SH} . R_{CN} is the nominal value of the local contact resistance, R_{C1kR}

is the random component of R_{C1k} and R_{C2kR} is the random component of R_{C2k} .

It will be assumed that the random components of the contact resistances are uncorrelated. From (A3), it follows that

$$\sum_{k=1}^n \frac{1}{R_{C1k}} = \sum_{k=1}^n \frac{1}{R_{CN} + R_{C1kR}} = \frac{1}{R_{CN}} \sum_{k=1}^n \frac{1}{1 + \frac{R_{C1kR}}{R_{CN}}} \quad (\text{A5})$$

Since the random component of the contact resistance is small compared to the nominal component, a power series expansion for each of the terms can be used to linearize the sum in (A5). Thus, by neglecting 2nd and higher-order terms in this expansion, we obtain

$$\sum_{k=1}^n \frac{1}{R_{C1k}} \approx \frac{1}{R_{CN}} \sum_{k=1}^n \left(1 - \frac{R_{C1kR}}{R_{CN}} \right) = \frac{n}{R_{CN}} \left(1 - \frac{1}{n} \sum_{k=1}^n \frac{R_{C1kR}}{R_{CN}} \right) \quad (\text{A6})$$

By repeating the power series expansion process, it follows that

$$\frac{1}{\sum_{k=1}^n R_{C1k}} \approx \frac{R_{CN}}{n} \left(1 + \frac{1}{n} \sum_{k=1}^n \frac{R_{C1kR}}{R_{CN}} \right) \quad (\text{A7})$$

A similar approach can be used to obtain the expression

$$\frac{1}{\sum_{k=1}^n R_{C2k}} \approx \frac{R_{CN}}{n} \left(1 + \frac{1}{n} \sum_{k=1}^n \frac{R_{C2kR}}{R_{CN}} \right) \quad (\text{A8})$$

Substituting equations (A2), (A7) and (A8) in equation (A1), it follows that

$$R \approx \frac{2R_{CN}}{n} + R_{SHN} + \frac{R_{CN}}{n^2} \left(\sum_{k=1}^n \frac{R_{C1kR}}{R_{CN}} + \sum_{k=1}^n \frac{R_{C2kR}}{R_{CN}} \right) + R_{SHR} \quad (\text{A9})$$

It follows from (A9) that the nominal value of the resistor is

$$R_N = \frac{2R_{CN}}{n} + R_{SHN} \quad (\text{A10})$$

and the random component of the resistor is

$$R_R \approx \frac{R_{CN}}{n^2} \left(\sum_{k=1}^n \frac{R_{C1kR}}{R_{CN}} + \sum_{k=1}^n \frac{R_{C2kR}}{R_{CN}} \right) + R_{SHR} \quad (A11)$$

If it is assumed that the random components of the contact resistance are identically distributed, it follows that

$$\frac{\sigma_{R_{C1kR}}^2}{R_{CN}} = \frac{\sigma_{R_{C2kR}}^2}{R_{CN}} = \sigma_{R_{CR}}^2 \quad (A12)$$

Since the random variable in (A11) are assumed to be uncorrelated, it follows from equations (A9), (A10), (A11), (A12) that the value of the resistance R can be approximated by

$$\sigma_R^2 = \sigma_{R_R}^2 \approx \frac{R_{CN}^2}{n^4} \left(2 \cdot n \cdot \sigma_{\frac{R_{CR}}{R_{CN}}}^2 \right) + \sigma_{R_{SHR}}^2 \quad (A13)$$

Or equivalently as

$$\sigma_R^2 \approx \frac{2R_{CN}^2}{n^3} \cdot \sigma_{\frac{R_{CR}}{R_{CN}}}^2 + R_{SHN}^2 \sigma_{\frac{R_{SHR}}{R_{SHN}}}^2 \quad (A14)$$

By dividing both sides of (A14) by R_N^2 , we can obtain an expression for the variance of the normalized resistance $\frac{R}{R_N}$, which takes the form

$$\sigma_{\frac{R}{R_N}}^2 \approx \frac{2R_{CN}^2}{n^3 \left(\frac{2R_{CN}}{n} + R_{SHN} \right)^2} \sigma_{\frac{R_{CR}}{R_{CN}}}^2 + \left(\frac{R_{SHN}^2}{\left(\frac{2R_{CN}}{n} + R_{SHN} \right)^2} \right) \sigma_{\frac{R_{SHR}}{R_{SHN}}}^2 \quad (A15)$$

Acknowledgement

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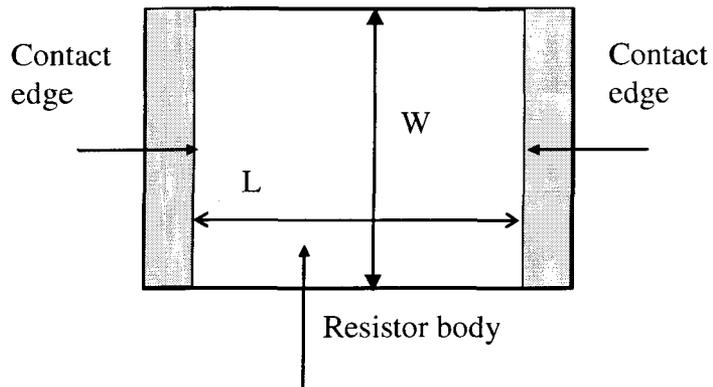


Fig.1. Homogeneous rectangular thin film resistor

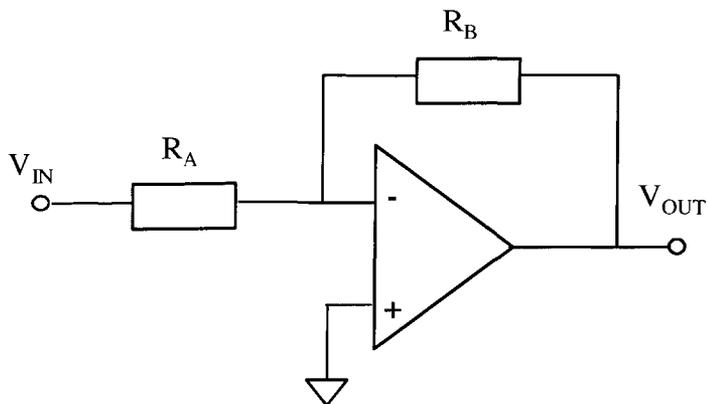


Fig.2. The basic resistor feedback amplifier

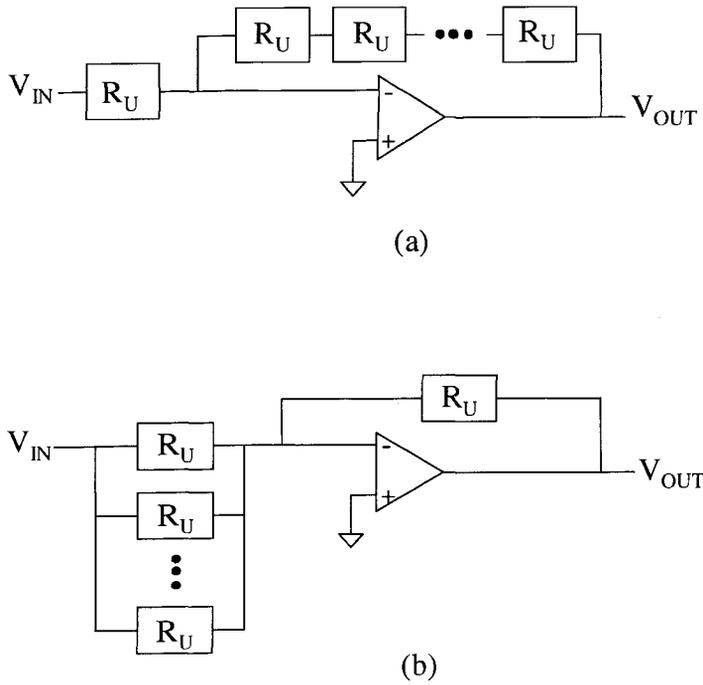


Fig.3. (a) Conventional series and (b) parallel area allocation strategies for amplifier

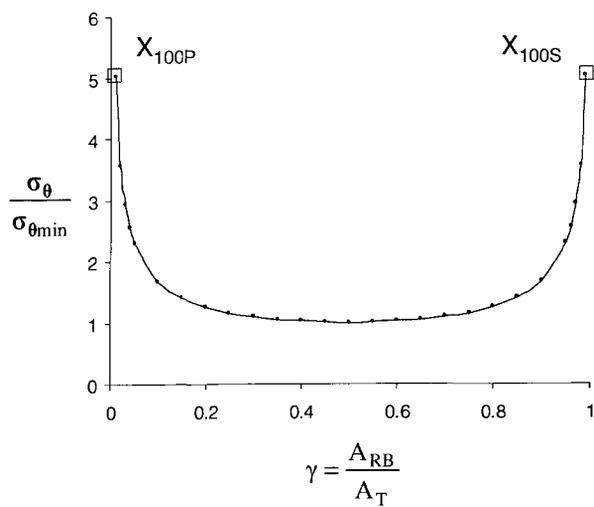
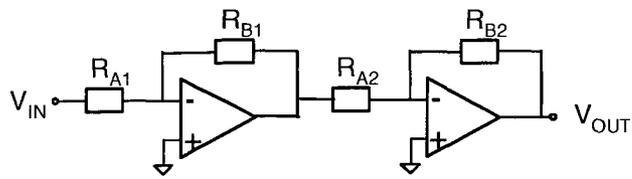
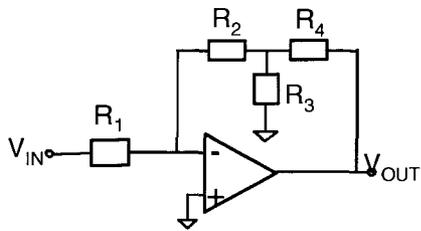


Fig.4. Effects of area partitioning on the normalized standard deviation



(a)



(b)

Fig.5. (a) Cascade amplifier (b) T-feedback network amplifier

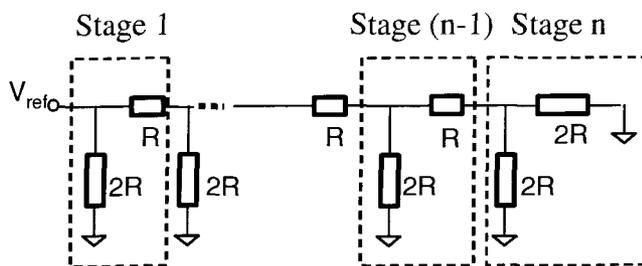


Fig.6. n-stage R-2R resistance ladder

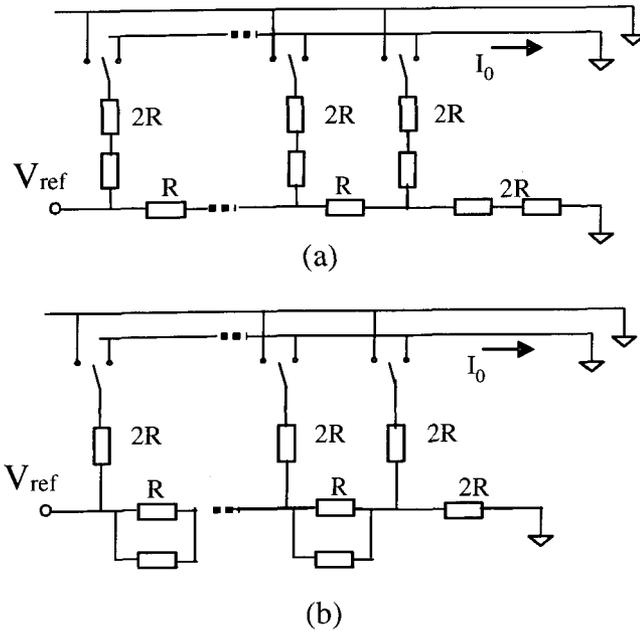


Fig.7. Conventional series and parallel area allocation strategies for R-2R ladder

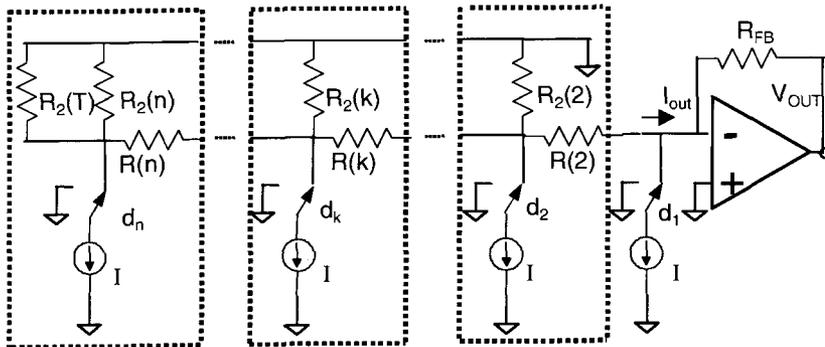


Fig.8. Equal-current R-2R DAC

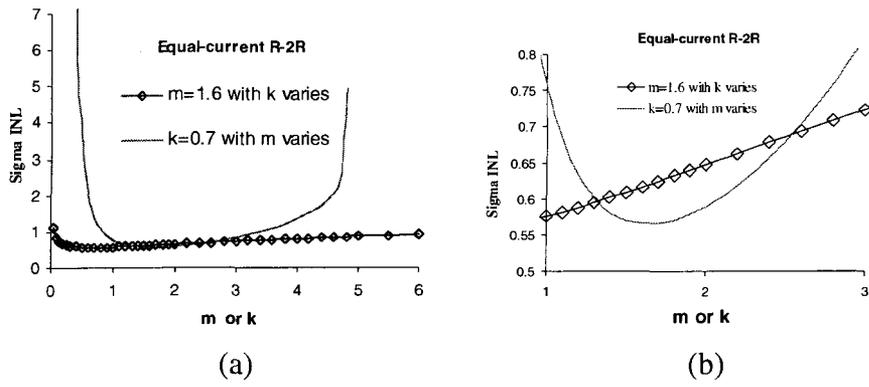


Fig.9. Sensitivity of standard deviation to m and k of an 8-bit equal-current R-2R DAC

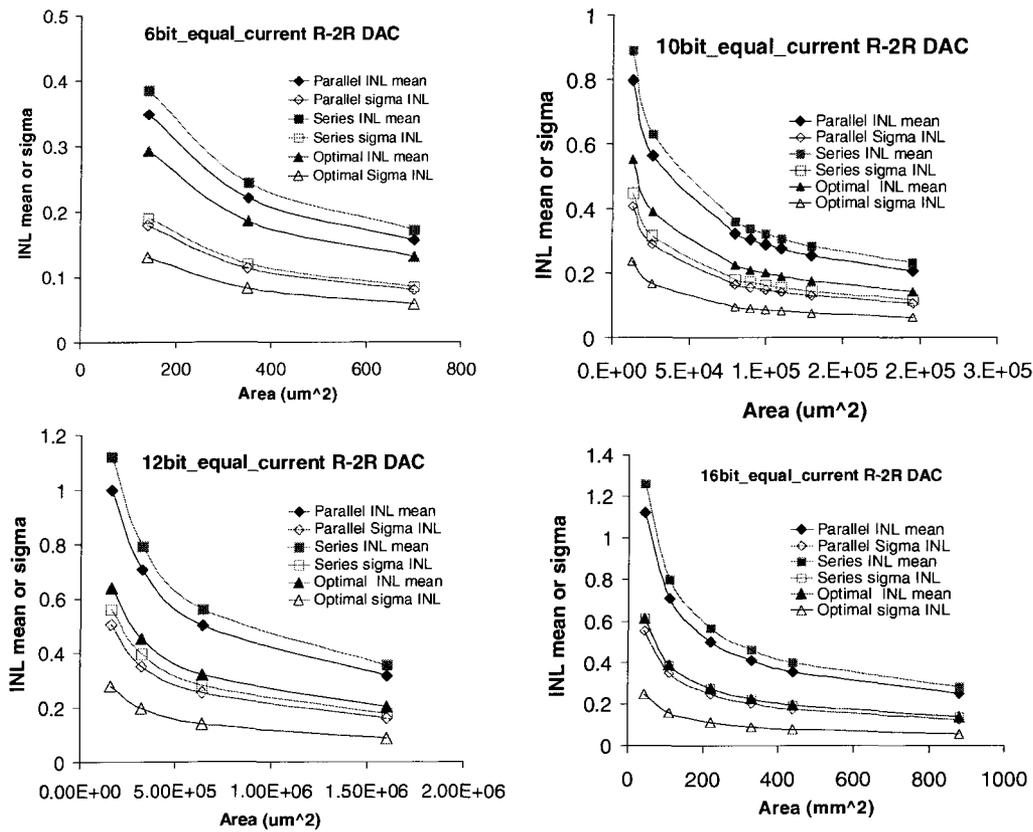


Fig.10. Mean and sigma of INL of equal-current R-2R DAC

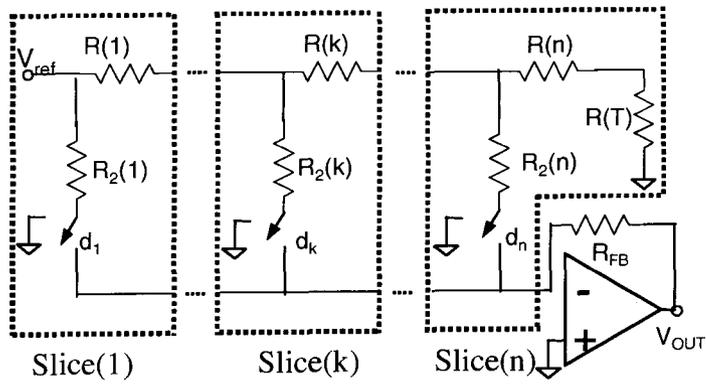


Fig.11. Binary-weighted-current R-2R DAC

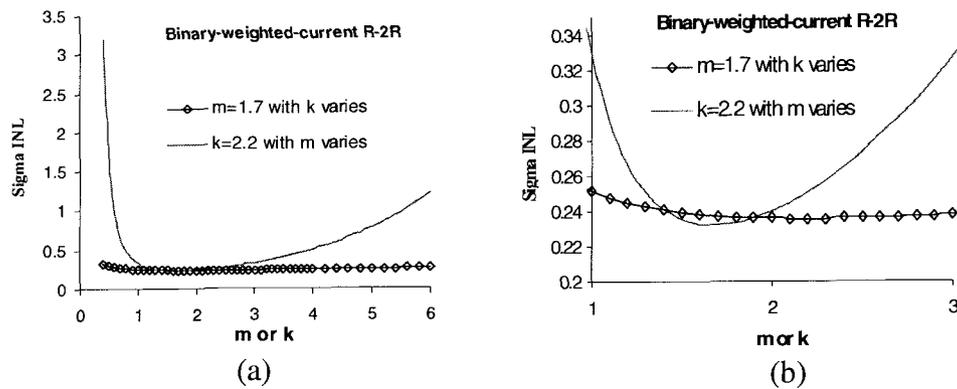


Fig.12. Sensitivity of standard deviation to m and k of an 8-bit binary-weighted current R-2R DAC

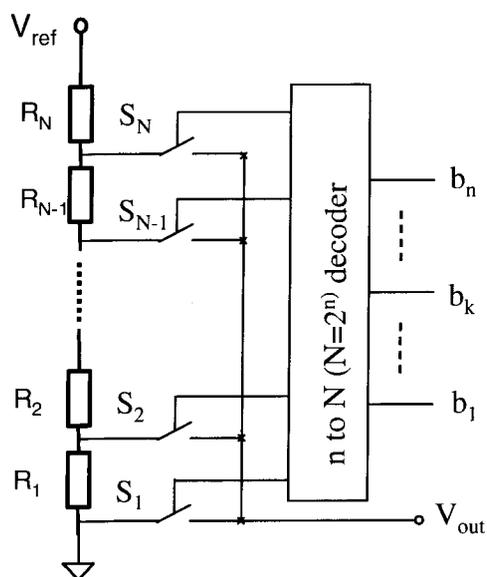
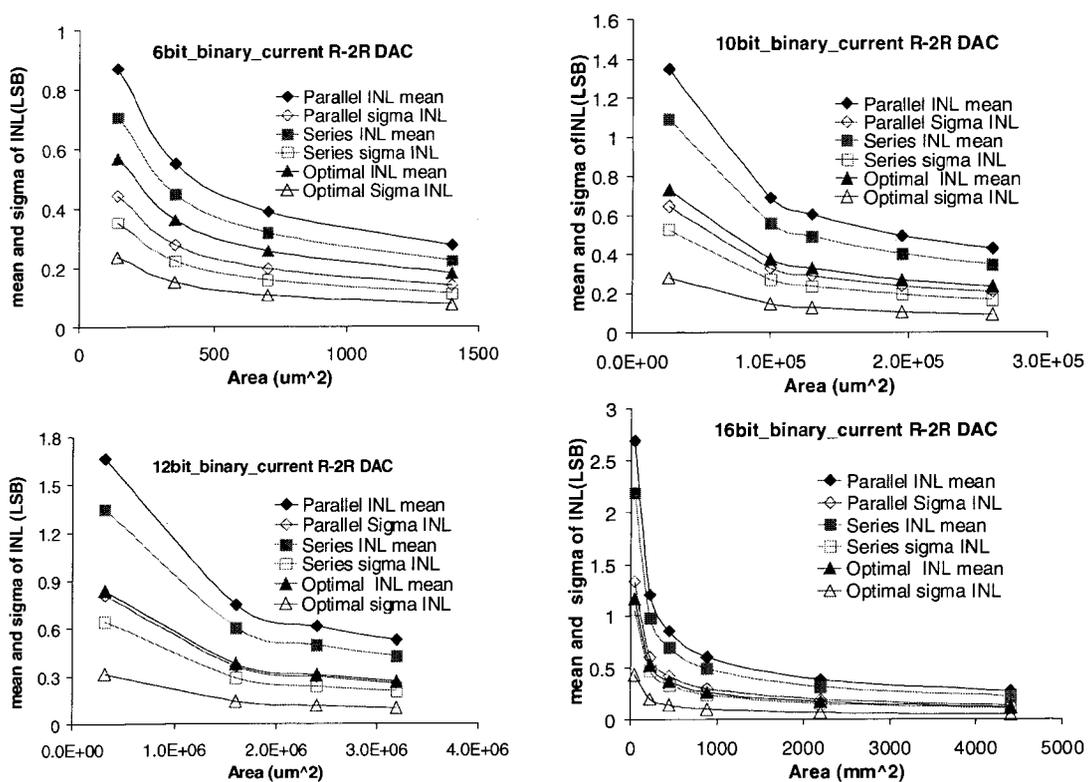


Fig.13. Mean and sigma of INL of binary-weighted-current R-2R DAC

Fig.14. Symbolic structure of resistor-string DAC

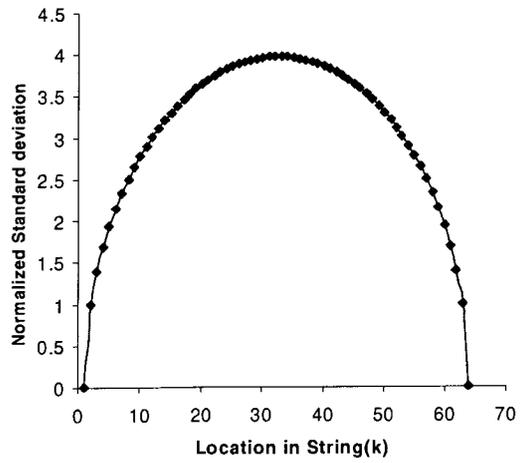


Fig.15. Plot of normalized standard deviation of INLk for N = 64

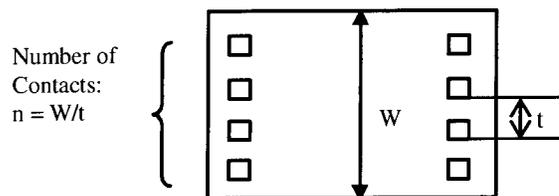


Fig.16. Symbolic layout of a resistor

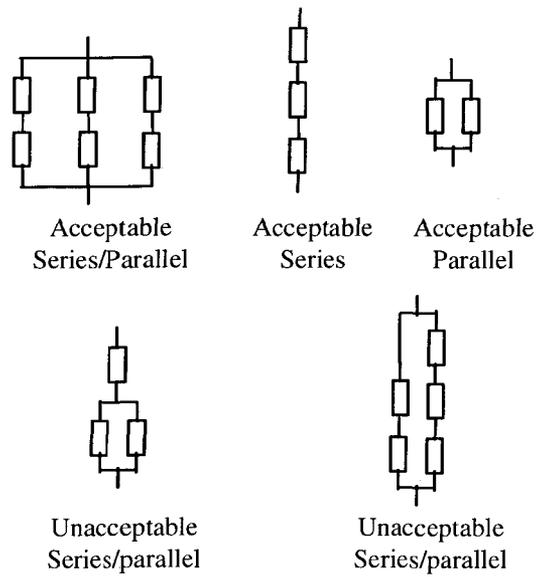


Fig.17. Examples of acceptable and unacceptable series, parallel and series/parallel implantation

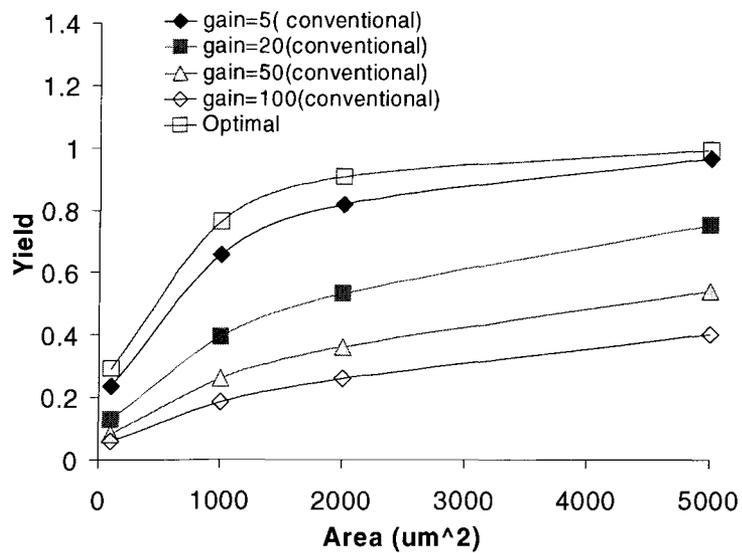


Fig.18. The yield of feedback amplifier

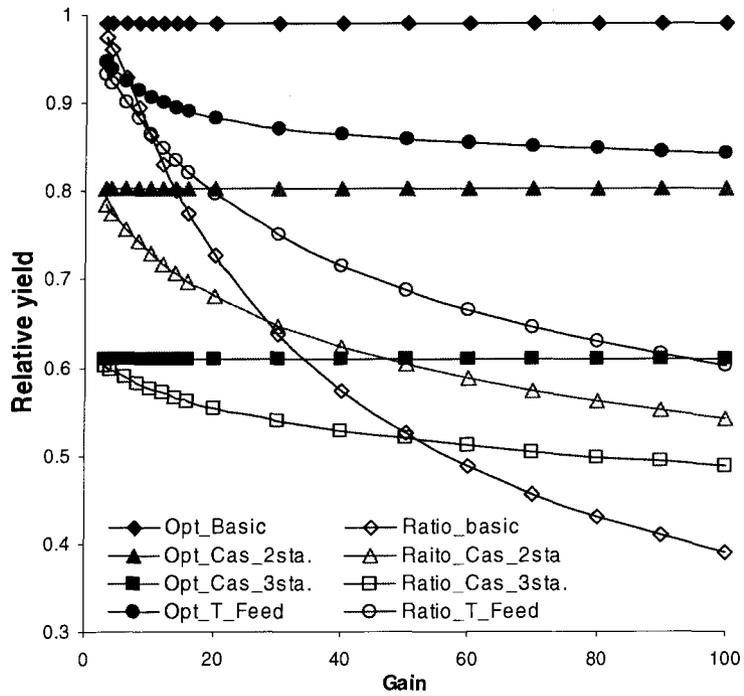


Fig.19. Yield of different configuration for feedback amplifier, “Opt” denotes optimal area allocation for a given structure, “Ratio” denotes a ratio-based area allocation strategy

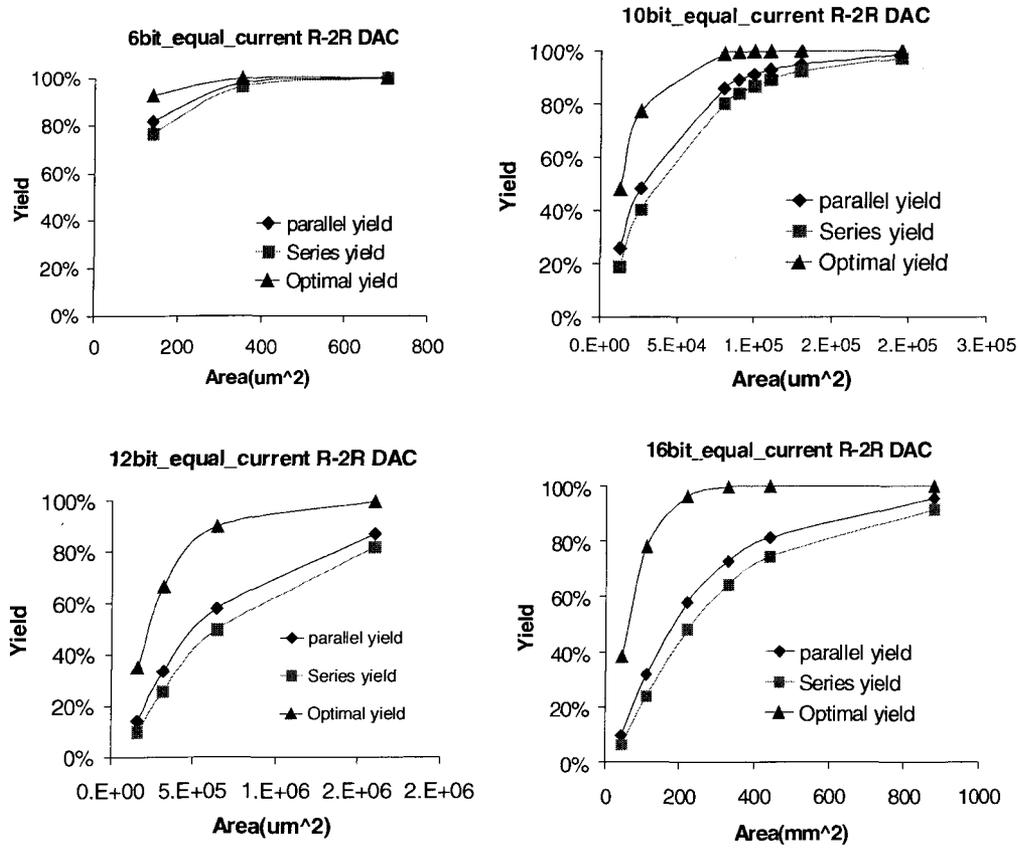


Fig.20. Yield of equal-current R-2R DACs

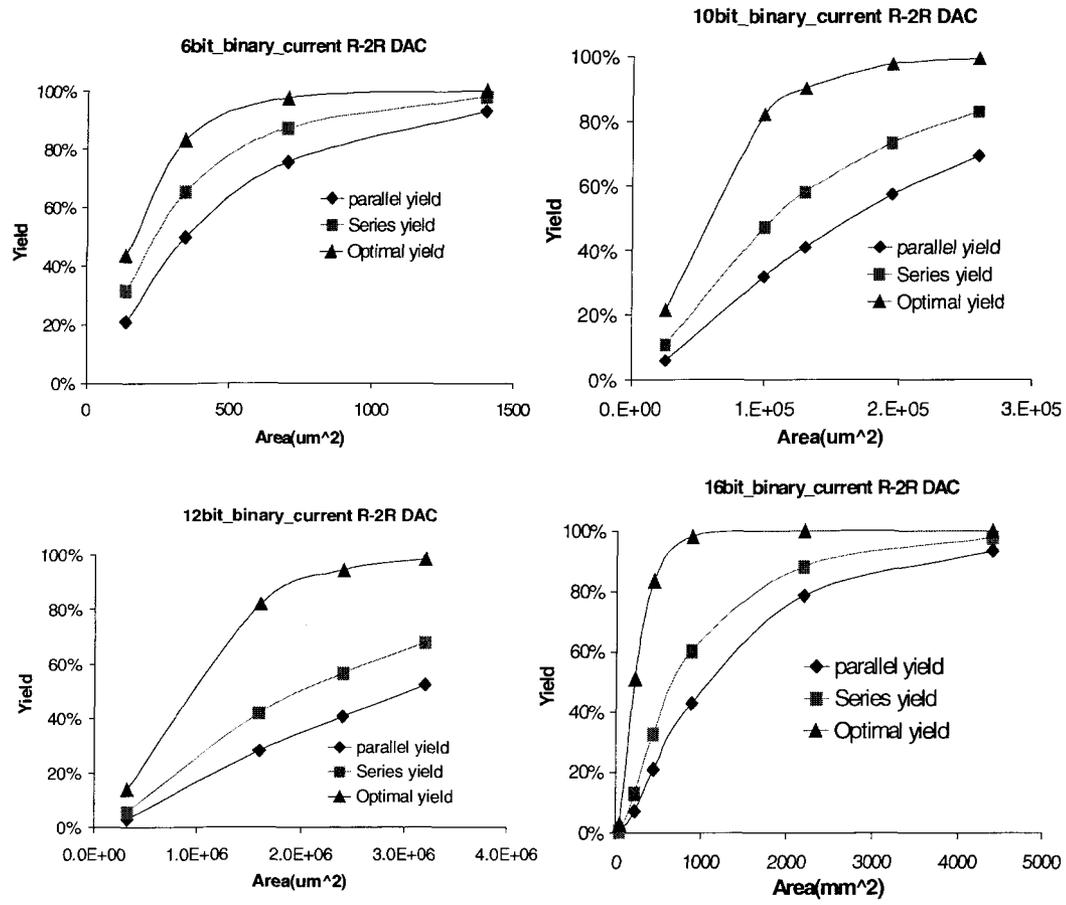


Fig.21. Yield of binary-weighted-current R-2R DACs

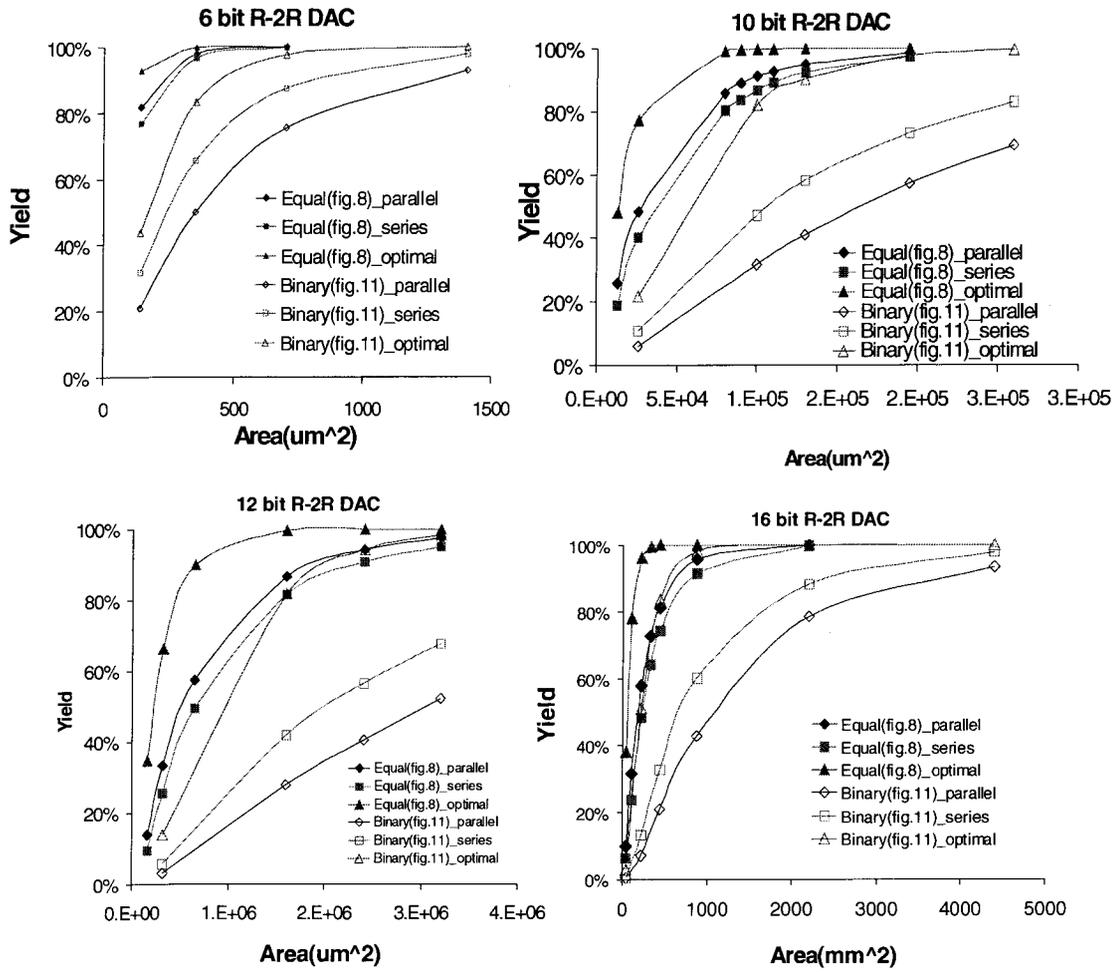


Fig.22. Yield of R-2R DACs

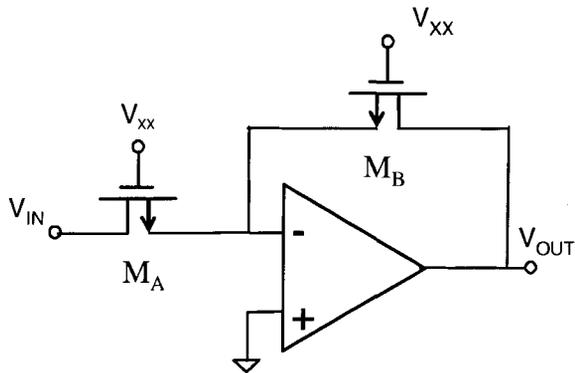


Fig.23. Basic transistor feedback amplifier

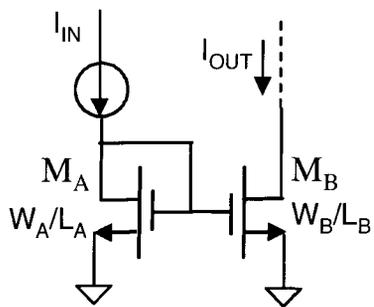


Fig.24. Basic current mirror

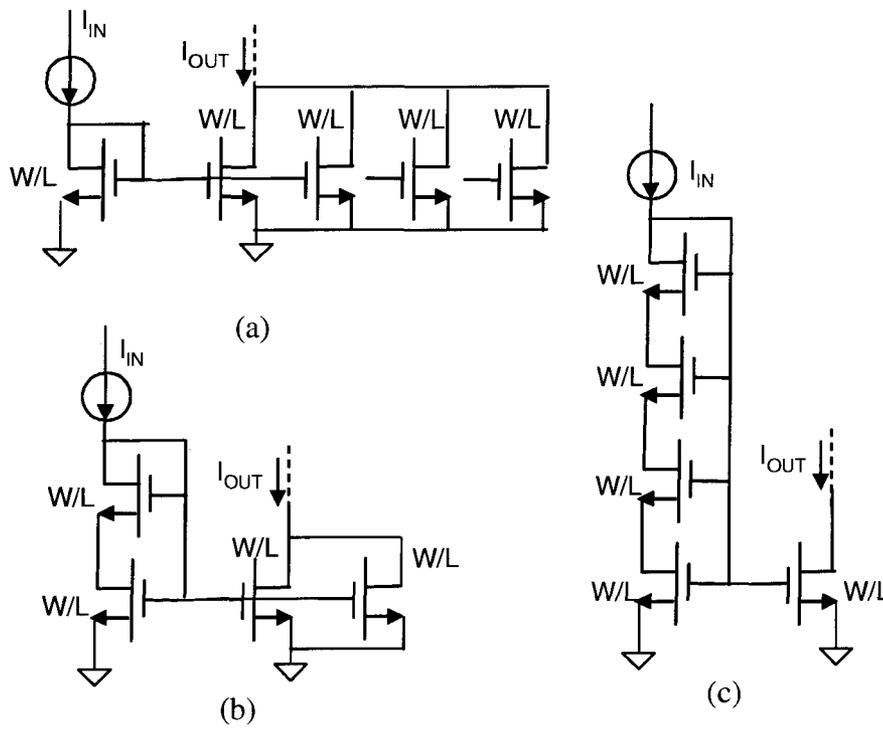


Fig.25. Different area allocation scheme for current mirrors with current gain of 4

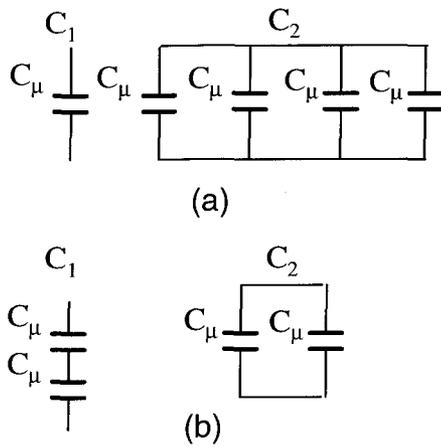


Fig.26. Different area allocation scheme for capacitor ratio of 4

CHAPTER 4. EXPERIMENTAL RESULTS FOR OPTIMAL AREA ALLOCATION OF PRECISION ANALOG TEST STRUCTURES

I. Introduction

To confirm the concept developed in Chapter 3, test structures for equal-current R-2R DACs and resistive feedback amplifiers were designed and laid out in 90 nm CMOS process. The Agilent HP4071A semiconductor parametric tester and a wafer probe station were used for the measurements. Source and Monitor Units (SMU) were used to sense and apply different voltages and currents. The SMUs have different precision and accuracy for different input and output ranges. The total number of independent SMUs used for these measurements is six. Two voltage sources and two voltage meters internal to the tester were also used. For testing on the wafer, a total 8 standard pad arrays with each pad array having 12 pads on each side were used for this experiment.

A test chip was designed that included R-2R resistor networks, resistor ratio networks and finite gain amplifiers. Both unsilicided p-doped polysilicon (PPOLY) and unsilicided p+ diffusion (POD) were used for the resistors. Resistor ratios in both the resistor ratio networks and the feedback elements in the finite gain amplifiers were fixed at 16. The area allocated to all test structures was selected to achieve a moderate yield since either a very large yield or a very small yield would not be practical in verifying the properties of the new structures with a relatively small number of test devices and measurements. . The total resistor area in each comparison group was the same.

The resistive feedback amplifier was designed for a high gain of 80 dB to minimize the effects of op-map gain on the closed loop gain. Considerable efforts were devoted to minimizing the adverse effects caused by via resistance and interconnect resistance, etc. All test structures were created so that the regions above and below each cell was the same. This necessitated the inclusion of dummy devices on the periphery of the test arrays

A test structure location diagram is shown in Fig.1 (a). An actual layout is shown in Fig. 1(b).

II. Resistive Feedback Amplifier

Fig. 2 shows a resistive feedback amplifier. For this test structure, the amplifier gain is (-16). The selected resistors are unsilicided p+ polysilicon resistors (PPOLY) and p+ diffusion resistors (POD).

A. Amplifier Design

The schematic of the amplifier is shown in Fig. 3. It is comprised of a two stage differential input and single-ended output amplifier with output buffer. Because our focus is on resistor ratios, the measurements were done at very low frequencies. Therefore, the speed requirements of the amplifier were greatly relaxed. High threshold voltage devices of this 90 nm CMOS process were used with a power supply voltage of around 2.5V. A modest gain boost was achieved by cascoding the n-channel input stage. A non-cascoded p-channel load was used for convenience of biasing the second stage since the threshold voltages in this process are rather large.

1). Simulation Results

Simulation results for the operational amplifier are shown in Fig. 4. The schematic simulation results show that the open-loop gain of the amplifier is 83.6 dB. The post-layout simulation results show that the open-loop gain of the amplifier is 80 dB.

B. Resistor Ratio Measurement

Resistor ratios were measured for both the conventional and the optimal area allocation schemes. The measurement setup for the resistor ratios is shown in Fig. 5. A standard four-point measurement was used to minimize the instrumentation resistance. In these measurements, current was applied between pins P_1 and P_5 . The voltage was measured between P_2 and P_3 , and between P_2 and P_4 . The resistor ratio is given by the equation

$$\frac{R_B}{R_A} = \frac{V_2 - V_1}{V_1} \quad (1)$$

1). Layout

The different area allocation schemes and layout configurations for a resistance ratio of 16 are shown in Fig. 6. A conventional area allocation scheme with a non-common-centroid configuration and with a common-centroid configuration are shown in Fig. 6(a) and Fig. 6(b), respectively. The common-centroid configurations are used to cancel gradient effects. An optimal area allocation scheme with a non-common-centroid configuration and with a common-centroid configuration are shown in Fig. 6(c) and Fig. 6(d), respectively. Since all the test structure has the same area, the size of the unit resistor changed from one test structure to the next because of a different number of unit resistors. The unit resistor size

for each of the eight unit cells in the optimal approach is $2.3 \mu\text{m} \times 0.46 \mu\text{m}$. The unit resistor size for each of the 17 unit resistors in the conventional series approach is $3.35\mu\text{m} \times 0.67\mu\text{m}$.

2). Simulation and Measurement Results

Schematic and post-layout simulation results for the resistor ratio network are shown in Table 1 and Table 2. The gain error is defined as the percentage gain difference between schematic and post-layout simulations. The common-centroid configuration is denoted as Cc. The non-Common-centroid configuration is denoted as Ncc. The conventional scheme is denoted as Con. The optimal scheme is denoted as Opt, the P type unsilicided diffusion resistor is denoted as POD, and the P type unsilicided polysilicon resistor is denoted as PPOLY.

Table 1 Schematic Simulation Results for Resistor Ratio

Configurations	Input Current(A)	Schematic Simulation Results		
		V_2-V_1 (V)	V_1 (V)	Ratio
Cc_Con_POD	100u	1.60058	0.100036	16.00004
Cc_Con_PPOLY	40u	1.81757	0.113598	16.00002
Cc_Opt_POD	400u	1.45496	0.090935	15.99995
Cc_Opt_PPOLY	200u	2.09397	0.130873	16.00002
Ncc_Con_POD	100u	1.60058	0.100036	16.00004
Ncc_Con_PPOLY	40u	1.81757	0.113598	16.00002
Ncc_Opt_POD	400u	1.45496	0.090935	15.99995
Ncc_Opt_PPOLY	200u	2.09397	0.130873	16.00002

The difference in the ratio from the nominal value of 16 for the schematic simulation is due to simulation and rounding errors and is approximately $\pm 0.00025\%$. This is one LSB at the 19-bit level. The post-layout simulation differences are somewhat larger and are due primarily to the parasitic interconnect resistance in the test structures. These errors are

systematic and could have been reduced with additional attention to layout. Emphasis in interpreting measurement results will be on variance, not on absolute accuracy, thus the modest systematic errors in the test structure are not of major concern.

Table 2 Post-layout Simulation Results for Resistor Ratio

Configurations	Input Current(A)	Post-Layout Simulation Results		
		V_2-V_1 (V)	V_1 (V)	Ratio
Cc_Con_POD	100u	1.61547	0.101190	15.96472
Cc_Con_PPOLY	40u	1.83924	0.115040	15.98727
Cc_Opt_POD	400u	1.47118	0.092158	15.96369
Cc_Opt_PPOLY	200u	2.11512	0.13231	15.98609
Ncc_Con_POD	100u	1.61552	0.100996	15.99588
Ncc_Con_PPOLY	40u	1.83926	0.114963	15.99871
Ncc_Opt_POD	400u	1.46991	0.092129	15.95500
Ncc_Opt_PPOLY	200u	2.11446	0.132284	15.98425

In order to characterize the yield performance of the different area allocation schemes on the resistor ratios, the standard deviation of the resistor ratio will be determined. The analytical, simulation and measurement results are shown in Table 3. In the derivations, it was assumed that $A_p/R_{\square N} = 0.01133\mu m$ for PPOLY resistor and $A_p/R_{\square N} = 0.02146\mu m$ for POD resistor.

The analytical results were obtained by extracting the process parameters from the provided model file and applying the method described in Chapter 3. Simulation results were obtained by running statistical simulations on the schematic of circuits. The small differences between the derived results and the simulation results are believed to be due to the limited accuracy of the statistical circuit simulation environment and possibly due to small differences in characterizing the mismatch statistics in the process.

Table 3 Standard Deviation of Resistor Ratio

Resistor String	Derivation	Simulation	Measurement	
	Sigma (Ratio)	Sigma (Ratio)	Mean (Ratio)	Sigma (Ratio)
Cc_Con_POD	2.19e-2	1.97e-2	16.15	2.07e-2
Cc_Con_PPOLY	1.17e-2	1.32e-2	16.05	1.31e-2
Cc_Opt_POD	1.10e-2	1.03e-2	16.00	0.92e-2
Cc_Opt_PPOLY	0.57e-2	0.55e-2	16.00	0.51e-2
Ncc_Con_POD	2.19e-2	1.97e-2	16.08	2.33e-2
Ncc_Con_PPOLY	1.17e-2	1.32e-2	15.98	1.08e-2
Ncc_Opt_POD	1.10e-2	1.03e-2	15.95	1.09e-2
Ncc_Opt_PPOLY	0.57e-2	0.55e-2	16.01	0.57e-2

The measurement sample size for each type of resistor string was 40, forming a total population of 320 test structures. Of these, 5 were defective so the actual population size were either 39 or 40, depending upon which test structures had defective devices. Each resistor string was measured at 20 μ A and 40 μ A. The measured ratio for each test device is the average of the resistance ratio measured at these two different current levels. After that, the average of the ratios and the standard deviation of the normalized ratios for each population was computed. From Table 3 it can be observed that the mean of all resistor ratios are closed to 16.

The measurement results are close to the analytical and simulation results. The random variation with the diffusion resistors is larger than that of poly resistor as is expected for this process. In particular, the measured ratio for Cc_Con_POD had a normalized standard deviation of 2.07e-2 compared to the 1.31e-2 of Cc_Con_PPOLY structure. More importantly, the optimal area allocation approach substantially reduces the random variation of the resistor ratio as predicted by the theoretical analysis, as evidenced by a small difference between the derived and measured standard deviations for each of the 8 different

test structures. These results also show that for the small physical dimensions of these test structures, the common-centroid layout does not provide a substantive advantage over that of non-common-centroid layout suggesting the extra layout complexity of a common-centroid layout is not justifiable for small structures in this process.

C. Resistive Feedback Amplifier

The measurement setup of the amplifier with a nominal closed-loop gain of 16 is shown in Fig. 7. There are four different configurations of resistive feedback amplifiers. These are summarized in Table 4. The total area for the resistors is the same in all 4 cases and identical to the sizes used for the resistor ratio test structures. The placements of the resistors are the same as used for the resistor-ratio test structures as well.

For each test structure, there are total nine pins. The designed values for the 3 inputs are $V_{amp+} = 1.3V$, $V_{dd} = 2.6V$, $V_{ss} = 0V$. The nominal value for the test points are $V_{b0} = 0.77V$, $V_{b1} = 1.6V$, $V_{b2} = 1.88V$. A DC sweep was performed on pin (V_{in1}), and voltage at pin (V_{in2}) and pin (V_{out}) were measured. The gain is defined to be the slope of the resulting transfer characteristic in the high-gain output region of the op-amp. This procedure removes amplifier offset.

1). Simulation and Measurement Results

The Post-layout transient simulation results are shown in Table 4. The input was swept from 1.28V to 1.3V at a temperature of 27°C. Two points were selected to determine the slope (gain). There was a slight curvature in the transfer characteristic thus limiting the accuracy of the simulated gain. However, these results were not intended for comparison

with the measured slope. They were used to confirm that the amplifier is working well and the gain is closed to 16.

Table 4 Post-layout Simulation Results of Closed-loop Amplifier Gain

Configuration	Output (mV)	Gain
FBAMP_CC_CON_POD	318.675	15.93375
FBAMP_CC_CON_PPOLY	319.173	15.95865
FBAMP_CC_OPT_POD	317.863	15.89315
FBAMP_CC_OPT_PPOLY	318.889	15.94445

One measurement of a resistive feedback amplifier with FBAMP_CC_CON_POD is shown in Fig. 8. According to the design, the input and output common-mode voltages are 1.3V. However, in Fig. 8, when input is 1.3V, the output is around 0.8 V, which indicates that there exists a large offset and the quiescent point is not closed to 1.3V. This offset was due to inadvertent inclusion of non-symmetric metal 1 interconnect across part of the input stage of the op-amp. This offset does not compromise the measurement of the amplifier gain but does require measuring the slope of the transfer characteristic in the high gain region of the op-amp. The high gain region for this feedback amplifier is around $V_{out} = 0.8V$, and in this region the slope is close to 16.

The sketch in Fig. 9 explains why the output does not have the correct gain at $V_{OQ}=1.3V$. It also shows that a gain of 16 can be obtained in an appropriate region. When the amplifier open loop gain is infinite, the closed-loop gain will be $1/\beta$. However, in practice, the open loop gain is finite, and the close-loop gain equals to $A_o/(1+\beta A_o)$ in the high gain region. Ideally, when the common-mode output voltage (1.3V) is in the middle, then it will have symmetric linear output swing. However, when the common mode output voltage shifts to the left as shown in the figure, then there is no longer a symmetric linear region around

1.3V. If the quiescent output voltage is around 0.8V, then there will be symmetrical voltage swing around 0.8.

In the high gain region, the data was fit to a line and the gain was determined. However, due to resolution limitation of the measurement instrument and some variation in the repeatability for multiple measurements, I have decided not to report the measurement results. The closed-loop gains were closed to the target value of 16 but measurement repeatability problems make it difficult to present meaningful variance data at this time.

III. Equal-Current R-2R DAC

A. 8-bit R-2R DAC

In order to compare the INL performance of an R-2R DAC with or without optimal area allocation scheme, an 8 bit R-2R DAC was investigated. The equal-current R-2R DAC was selected because it is insensitive to switch impedance in the R-2R ladder thus making measurements on a test structure easier to make.

The measurement setup is shown in Fig. 10 where there are total 10 pins. One pin was connected to the substrate. Pins P_9 and P_1 were connected to ground. Because of the limited number of SMUs, the current was sequentially injected into each pin from P_2 to P_8 and the output current corresponding to each binary input code, I_{out} , was measured. Superstition of the output current corresponding to the full range of digital input codes was obtained and the INL was then calculated.

Because of the non-negligible difference in grounds introduced by two SMUs at pin P_1 and P_9 , each measurement was repeated with these two SMUs exchanged and the average of the output currents was used to determine the output.

1). Layout

The R-2R networks were restricted to P-type unsilicided polysilicon resistors. Two test structures were created. One was with the conventional series area allocation and the other with a near-optimal area allocation. Both were comprised of 15 resistors and the total resistor area was the same in both structures. The number of unit cells and correspondingly the size of the unit cells differed between the two structures. In the conventional series structure, there were 20 unit cells, each of size $7.3\mu\text{m} \times 0.73\mu\text{m}$. In the near-optimal structure, there were 55 unit cells, each of size $4.4\mu\text{m} \times 0.44\mu\text{m}$.

In Table 5, key parameters of the 8-bit R-2R DAC test structures are listed. Because the MSB current is directly injected into the inverting input of the amplifier, there are actually only seven stages.

Table 5 Layout Parameters for 8-bit R-2R DAC

Configuration	Number of unit cells	Unit cell size (μm^2)	Active area (μm^2)	Total area (μm^2)
Near-Optimal	55	4.4 x 0.44	106.48	78 x57
Conventional series	20	7.3 x 0.73	106.58	85 x64

In Table 6, the number of unit resistors used for the implementation of each resistor of the R-2R DAC are listed. Although the geometric decrease in the scaling of area from the MSB to the LSB theoretically provides optimal yield for a given area, there are challenges associated with continued scaling of area if the number of bits of resolution is large. It was shown in Chapter 3 that the major benefit in performance for the equal current R-2R DAC is obtained by scaling of the few MSB slices and that near optimal performance can be obtained

if the latter LSB slices are all equally sized and realized with a small number of standard unit resistors.

In this work, only near-optimal area allocation scheme and conventional series area allocations are compared.

Table 6 Implementation of Resistors for 8-bit R-2R DAC

		2R (# of unit cells)	R (# of unit cells)	A_{2R}/A_R	A_{MSB}/A_{MSB-1}
Near-Optimal Scheme	MSB(1st)	9	18	0.5	2.25
	2nd	4	8	0.5	4
	3rd	1	2	0.5	1
	4th	1	2	0.5	1
	5th	1	2	0.5	1
	6th	1	2	0.5	0.75
	LSB(7th)	2(R)	2	1	N/A
Conventional Series Scheme	MSB(1st)	2	1	2	1
	2nd	2	1	2	1
	3rd	2	1	2	1
	4th	2	1	2	1
	5th	2	1	2	1
	6th	2	1	2	1.5
	LSB(7th)	1(R)	1	1	N/A

The common-centroid layout configuration for the near-optimal scheme is depicted in Fig. 11. The MSBs were implemented with 9 unit cells connected in a 3x3 series/ parallel configuration to implement the “2R” resistor and 18 unit cells were connected in a 3x6 series/parallel configuration to implement the “R” resistor for the MSB slice. For the MSB-1 slice, 4 unit resistors were connected in a 2x2 series/ parallel configuration to implement the “2R” resistors and 8 unit resistors connected in a 2x4 series/parallel configuration were used to implement the “R” resistor. Since the MSB stages are more significant contributors to the performance, for the convenience of layout, only the first two or three MSB stages were

configured in common-centroid fashion. The common-centroid layout for the conventional approach is depicted in Fig. 12.

Although the test structures of near-optimal area allocation were implemented as shown in Table 6, it will be shown later that the yield for this approach is not very near to that of the optimal approach. There may exist some other ways of implementation so that the yield can be even nearer to the optimal approach.

2). Simulation and Measurement Results

In Table 7, the post-layout simulation results for 8-bit equal-current R-2R DAC is listed. A current of 1mA is injected to one pin at one time and the output is measured. Based on the data, the INL was computed.

For these test structures, the INL of R-2R DAC were evaluated at the 9-bit level. Good part was defined to be one with INL less than or equal to 0.5 LSB. From the table, it can be seen the nominal INL values are less than 0.05 LSB, which are much smaller than 0.5 LSB. Therefore, if the measured INL is large than 0.5LSB, it is mostly due to the random variations of INL.

Table 7 Post-layout Simulation Results of 8 bit R-2R DAC

Current (uA)	Near-Optimal	Conventional Series
1 st	1000	1000
2 nd	500.008	499.935
3 rd	250.038	249.97
4 th	125.027	124.996
5 th	62.5323	62.5189
6 th	31.2807	31.2683
7 th	15.6548	15.6355
8 th	7.83608	7.81902
INL (LSB at 9-bit level)	0.035903	0.021275

In Table 8, the statistical simulation results of 8-bit equal-current R-2R DAC with INL less than 0.5 LSB (9-bit level) is presented. A C++ program is written to do the computation.

Table 8 Statistical Simulation Results of 8 bit R-2R DAC

	Active Area(μm^2)	Mean of INL (LSB)	Sigma of INL (LSB)	Yield
Conventional Series	110	0.3677	0.1872	78.69%
Optimal	110	0.2514	0.1105	97.12%
Near-optimal	106.48	0.2881	0.1285	93.26%

It can be observed from the table that the near-optimal area allocation scheme greatly improves the yield compared to the conventional series approach. The near-optimal area allocation does degrade the yield compared to what achievable with the optimal approach.

The measurement results of the 8-bit R-2R DAC are shown in Table 9. The current applied at each individual input was $20\mu\text{A}$. The sample size for each structure is 40 samples and measurements from all 40 samples were included in the statistical results.

Table 9 Statistical Measurement Results of 8 bit R-2R DAC

	Mean of INL (LSB)	Sigma of INL(LSB)	Yield
Near-Optimal	0.3605	0.1270	85%
Conventional Series	0.4003	0.1685	75%

From the table, we observed that for both approaches, the standard deviations of INL are close to the expected value. In particular, the measured INL of the near-optimal structure had a standard deviation of 0.1270 LSB compared to the 0.1285 LSB predicted by simulations of the conventional series structure. However, the mean of the INL for the conventional approach is a little bit higher than the expected value shown in Table 8. This was due to a systematic error in the layout of the LSB part of the array that can be removed

with a more careful layout. Nevertheless, the good match of the standard deviation of the INL confirmed that the MSB stages are the major contributors of the random variations of INL.

B. 4 MSB Stages of 8-bit R-2R DAC

It was shown in Chapter 3 that the major benefit in performance of R-2R DACs is from the area scaling of the first few MSB stages. To further validate this observation, 4 MSB stages of what would be an 8-bit DAC were implemented. The circuit schematic of a test circuit comprised of these 4 MSB stages along with the measurement setup are shown in Fig. 13. The measurement procedure was the same as what was described in last section except for a reduction number of input currents from 7 to 3.

1). Layout

Layouts of the 4 MSB stages are the same as the first 4 MSB stages of what would be a full 8-bit DAC and are identical to what was shown in Fig. 11 and Fig. 12. Two test structures were created. One was with the conventional series area allocation and the other with a near-optimal area allocation. Both were comprised of 7 resistors, but the total resistor area for each structures was not the same. Note that more total area was allocated to the near-optimal area allocation than the conventional series structure. This correctly reflects the increased area allocated to the 4 MSB stages in an 8-bit structure if the total resistor area for the 8-bit structures were to be the same. The number of unit cells and correspondingly the size of the unit cells differed between the two structures. In the conventional series structure, there were 8 unit cells, each of size $7.3\mu\text{m} \times 0.73\mu\text{m}$. In the near-optimal structure, there

were 43 unit cells, each of size $4.4\mu\text{m} \times 0.44\mu\text{m}$. Key layout parameters of the test structures are listed in Table 10.

Table 10. Layout Parameters for 4 MSB Stages

Configuration	Number of unit cells	Unit cell size (μm^2)	Active area (μm^2)	Total area (μm^2)
Near-Optimal	43	4.4 x 0.44	83.248	68 x 57
Conventional Series	8	7.3 x 0.73	42.632	64 x 41

2). Simulation and Measurement Results

In Table 11, post-layout simulation results of the static performance for the 4 MSB stages are shown. In these simulations, the random variation effects of the resistors are excluded.

In Table 12, the statistical simulation and measurement results for this R-2R DAC are presented. 40 test cells for both the near-optimal structure and the conventional series structure were measured to obtain this data and all measured data was included in this statistical characterization. The forced current for each individual input of the DAC was 20uA. The INL at 9-bit level were computed using the same method discussed in the previous section. Good part was defined to be one with INL less than or equal to 0.5 LSB. Since the contribution of the LSB stages to the random variation of INL is negligible, the simulation results for this circuit are the same as that in Table 8 and are repeated in Table 12.

Table 11 Post-layout Simulation Results of 4 MSB Stages

Current (uA)	Near-Optimal	Conventional Series
1st	1000	1000
2nd	500.031	499.975
3rd	250.032	249.985
4th	125.029	125.003
INL(LSB at 9bit level)	0.0154874	0.0330228

Table 12 Statistical Simulation and Measurement Results of 4 MSB Stages

	Measurement			Simulation		
	Mean (INL)	Sigma(INL)	Yield	Mean (INL)	Sigma(INL)	Yield
Near-Optimal	0.2783	0.1304	92.5%	0.2881	0.1285	93.26%
Con. Series	0.3980	0.1797	72.5%	0.3677	0.1872	78.69%

It can be observed from this table that the measured data closely matches the predicted performance. In particular, the measured INL of the near-optimal structure had a standard deviation of 0.1304 LSB compared to the 0.1285 LSB predicted by simulations of the conventional series structure. The yield of the near-optimal area allocation structure is substantially higher than that of the conventional series area allocation.

IV. Conclusions

Test structures for optimal and near-optimal area allocation schemes and conventional area allocation schemes for several practical applications including rationed resistors, finite gain amplifiers, and R-2R DACs have been designed and fabricated in a 90nm CMOS process and extensive measurements have been made to validate the yield improvement potential for the optimal area allocation approach. Optimal area allocation strategies can provide a significant reduction in local random variations of key specifications of several widely used matching-critical circuits. This reduction in local random variations provides a significant yield improvement when compared to conventional widely used component ratio based area allocation schemes.

Acknowledgement

This work was supported in part by Freescale Semiconductor, the Semiconductor Research Corporation (SRC), and the National Science Foundation (NSF).

mm1	mm2	mm3	mm4	mm5	mm6	mm7	mm8
FBAMP CC_CON POD	FBAMP CC_CON PPOLY	FBAMP CC OPT POD	FBAMP CC OPT PPOLY	FBAMP NCC_CON POD	FBAMP NCC_CON PPOLY	Cc_CON POD	NCC_CON POD
R-2R 4MSB Con_Series CC_1	R-2R 4MSB Con_Series NCC	R-2R 4MSB Near-Opt CC_1	R-2R 4MSB Near-Opt CC_2	R-2R 4MSB Near-Opt NCC	FBAMP NCC OPT POD	CC_CON PPOLY	NCC-CON PPOLY
R-2R 8-bit Con_Series CC_1	R-2R 8-bit Con_Series NCC	R-2R 8-bit Near-Opt CC_1	Unit_gain Amp	R-2R 8-bit Near-Opt NCC	FBAMP NCC OPT PPOLY	CC_OPT POD	NCC_OPT POD
						CC_OPT PPOLY	NCC_OPT PPOLY

FBAMP Feedback Amplifier
 CC Common-centroid
 CC_1 Common-centroid configuration 1
 CC_2 Common-centroid configuration 2
 NCC Non-Common-centroid
 CON Conventional
 Near-Opt Near-optimal
 Opt Optimal
 POD Unsilicided P+ diffusion resistor
 PPOLY Unsilicided P+ polysilicon resistor

Fig.1 (a) The test structure location diagram

mm1 mm2 mm3 mm4 mm5 mm6 mm7 mm8

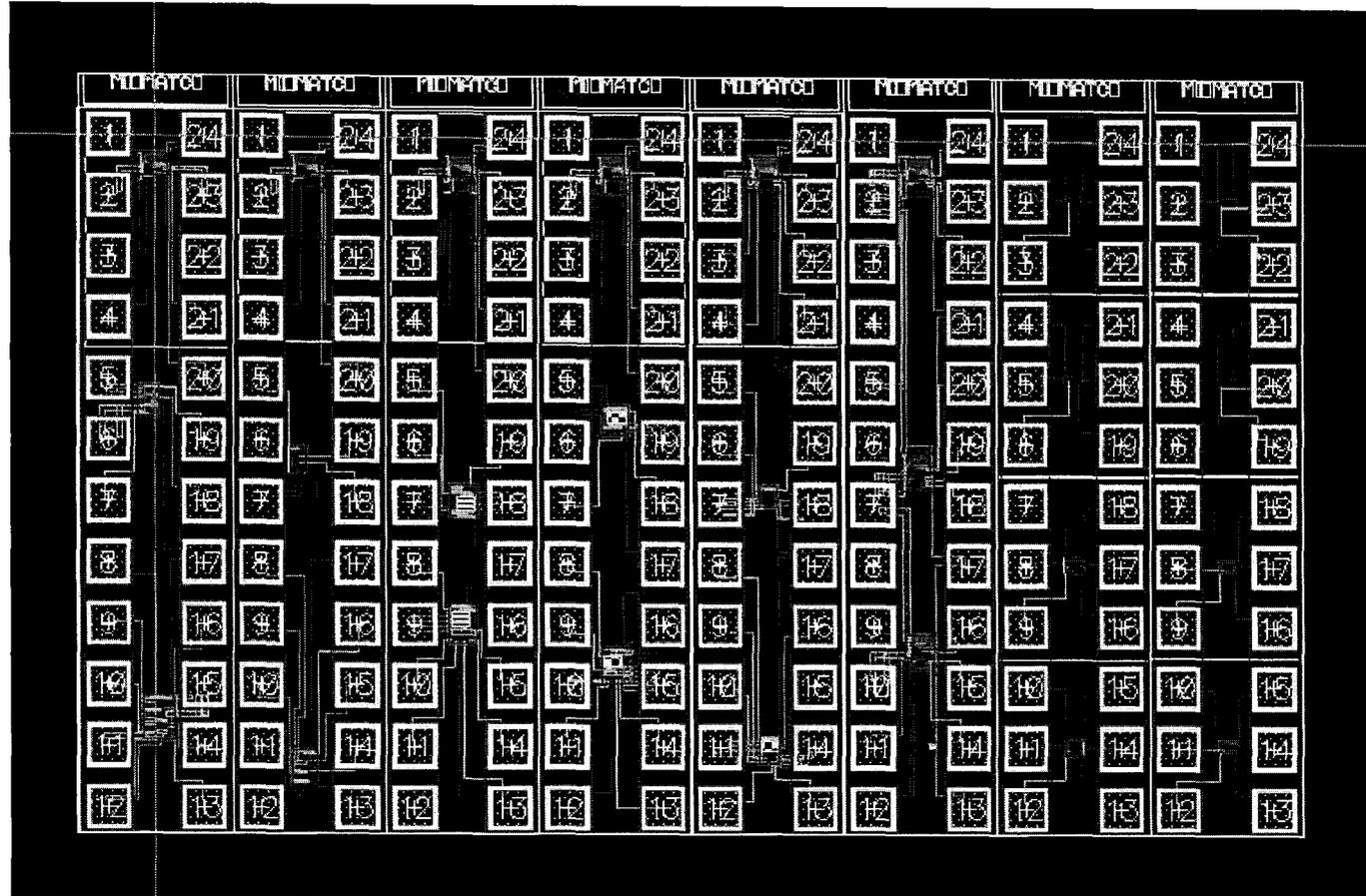


Fig.1(b) The layout of overall test structures

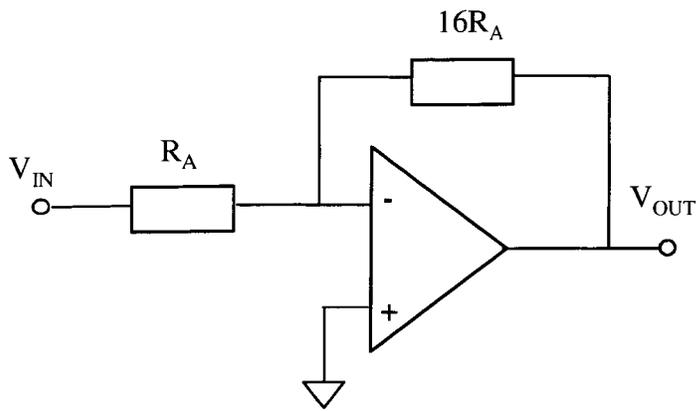


Fig.2. The basic resistor feedback amplifier with gain of (-16)

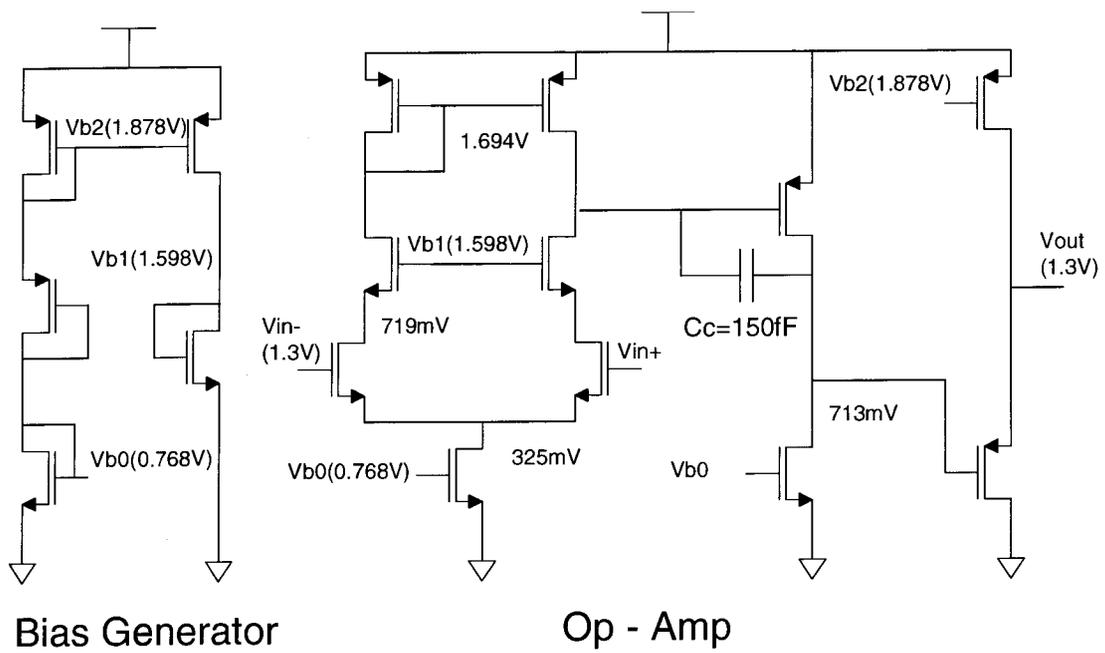
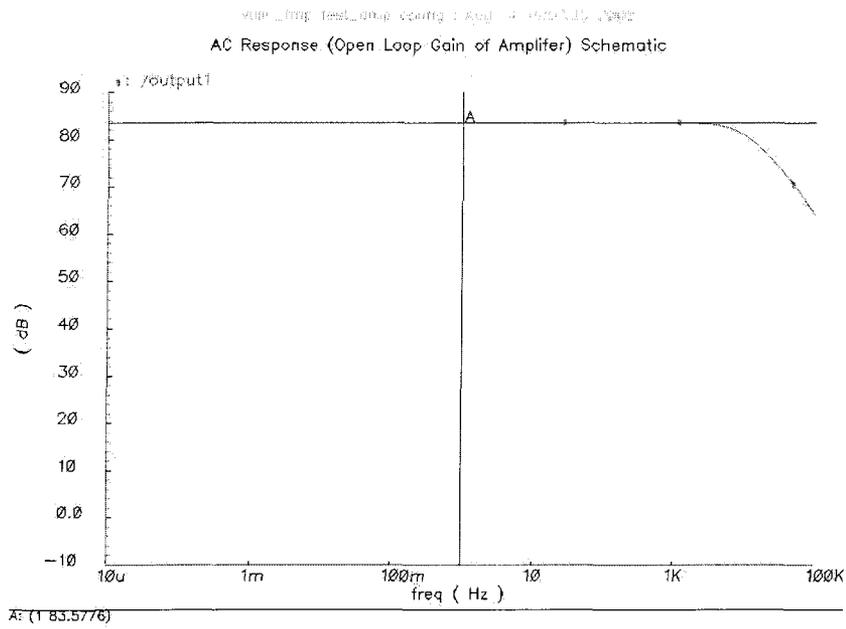
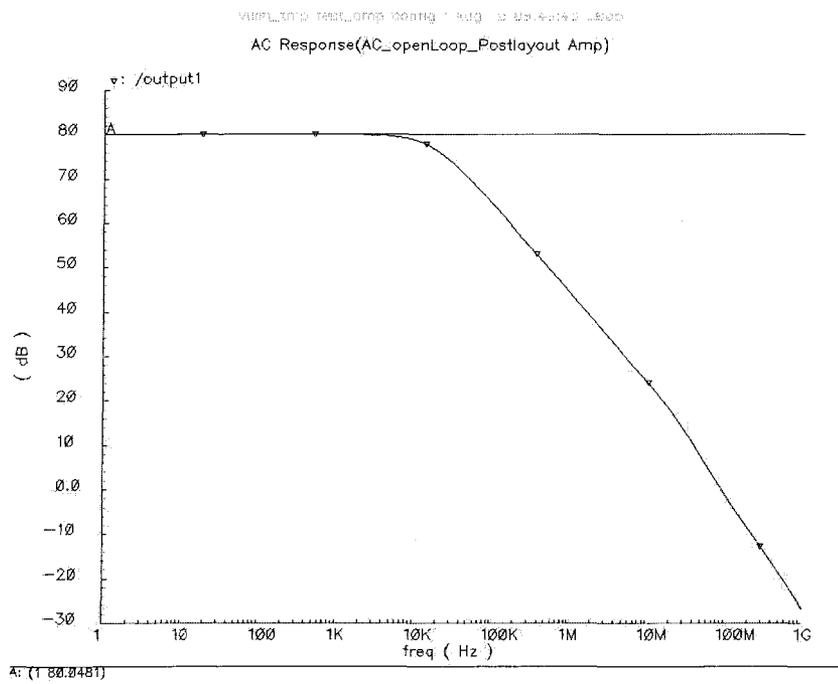


Fig.3. The amplifier with bias generator



(a)



(b)

Fig. 4. Open-loop gain of amplifier (a) schematic simulation; (b) post layout simulation

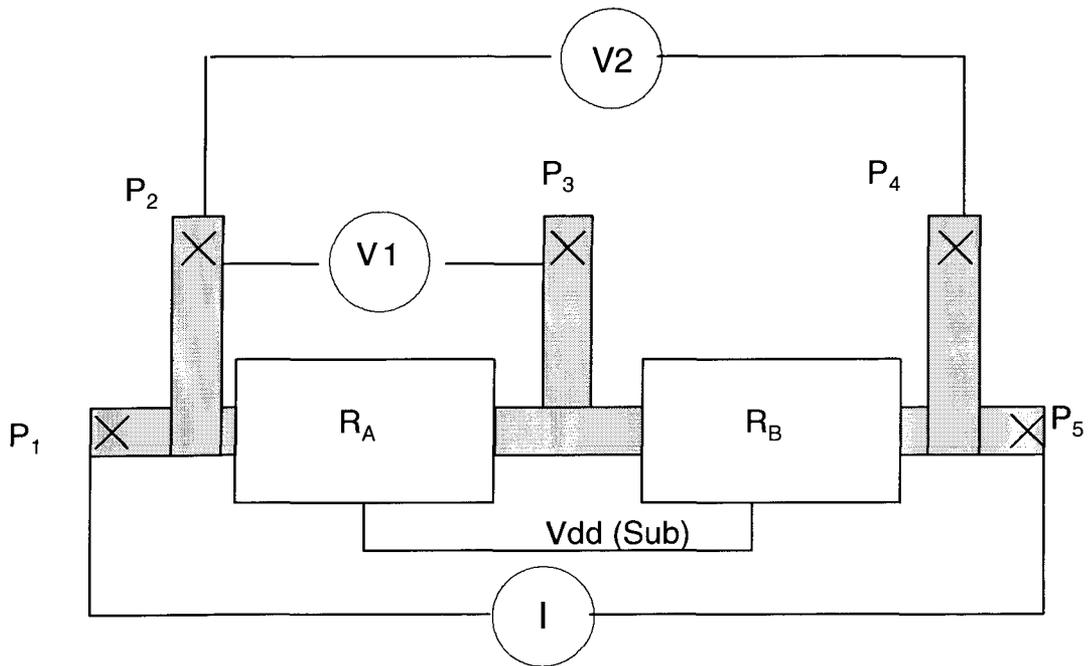
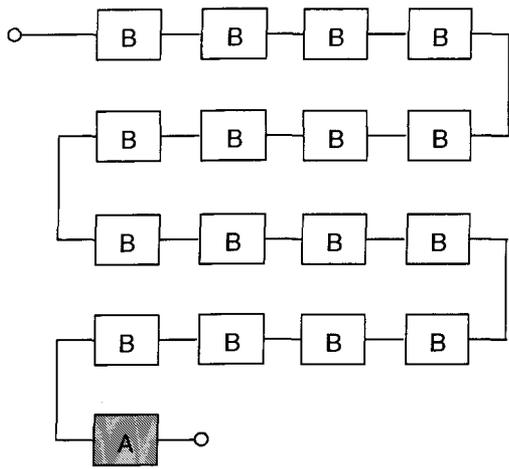
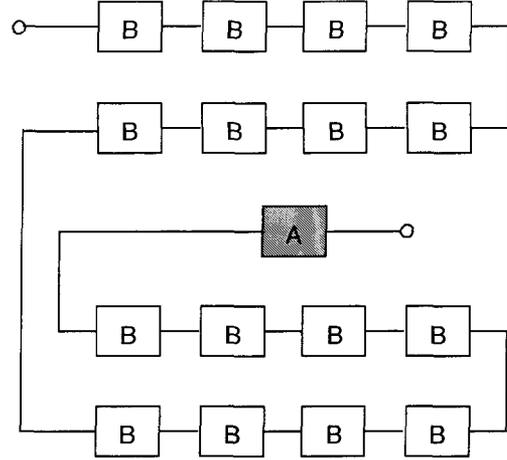


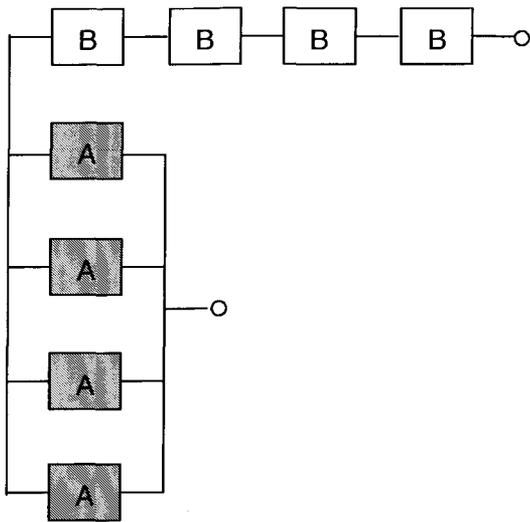
Fig.5. Four-point measurement of resistance



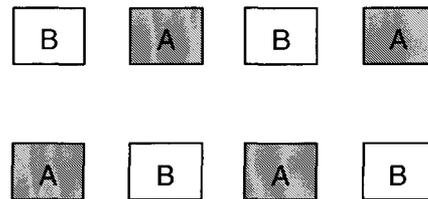
(a)



(b)



(c)



(d)

Fig.6 Conventional series scheme with (a) non-common-centroid configuration; (b) common-centroid configuration; Optimal scheme with (c) non-common-centroid configuration; (d) common-centroid configuration for resistor ratio of 16

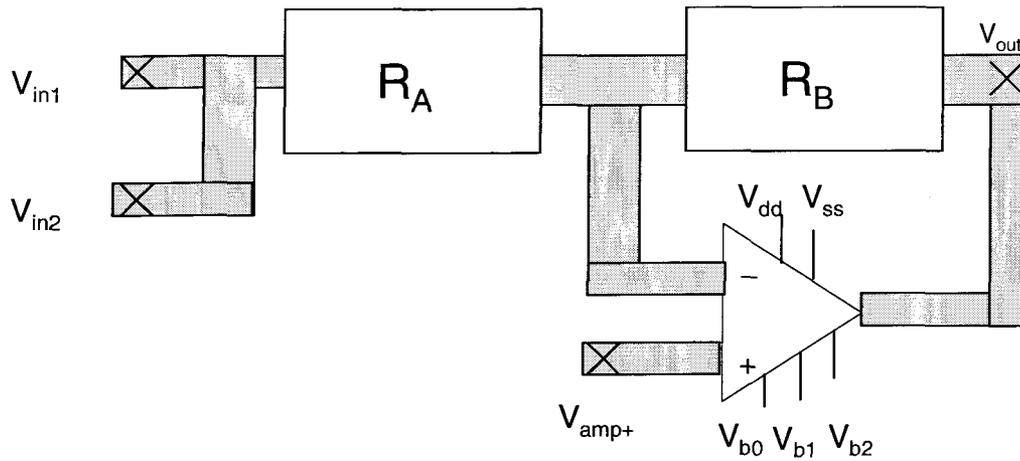


Fig.7 Measurement of amplifier closed-loop gain

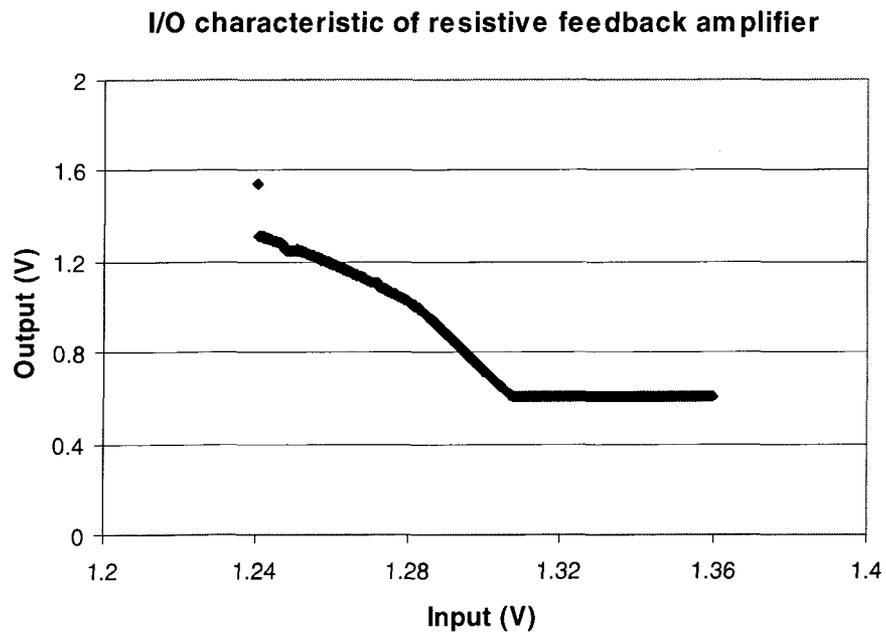


Fig.8 Input and output of an amplifier with conventional, poly resistor, common-centroid configuration

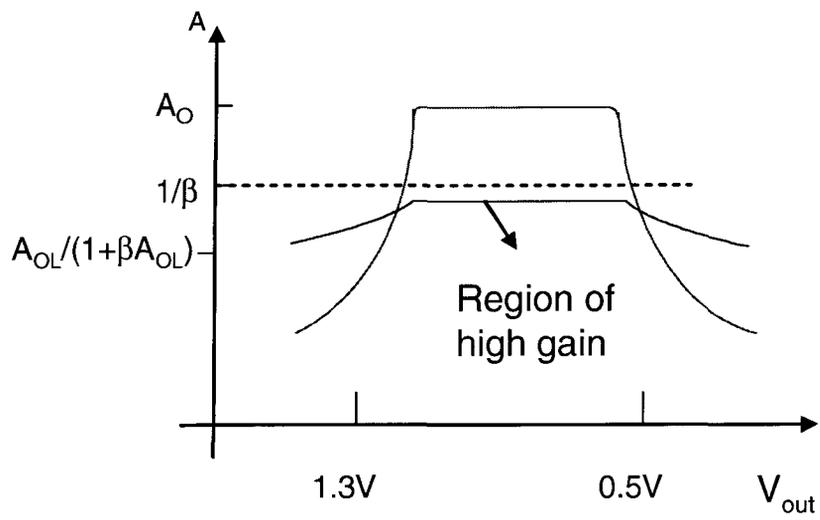
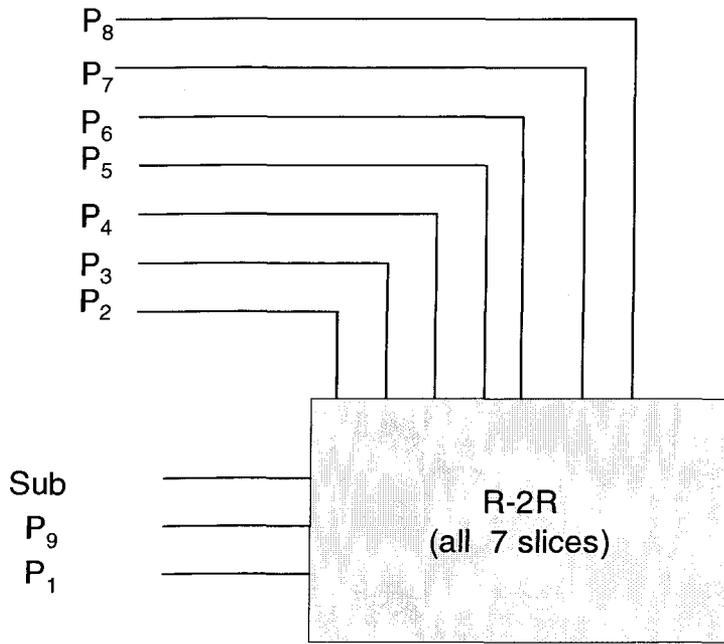
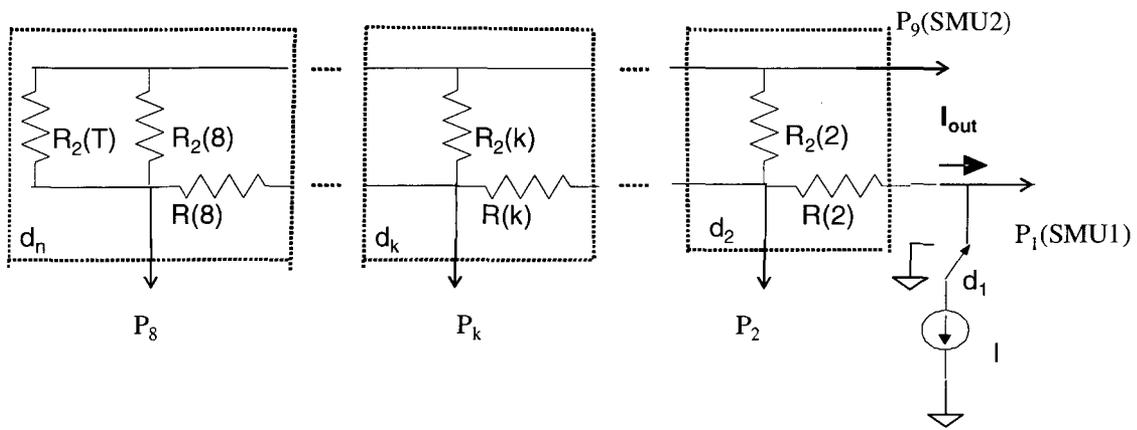


Fig. 9 The closed-loop gain and current characteristic for an amplifier



(a)



(b)

Fig. 10 (a) Measurement setup and (b) schematic of 8 bit equal-current R-2R DAC

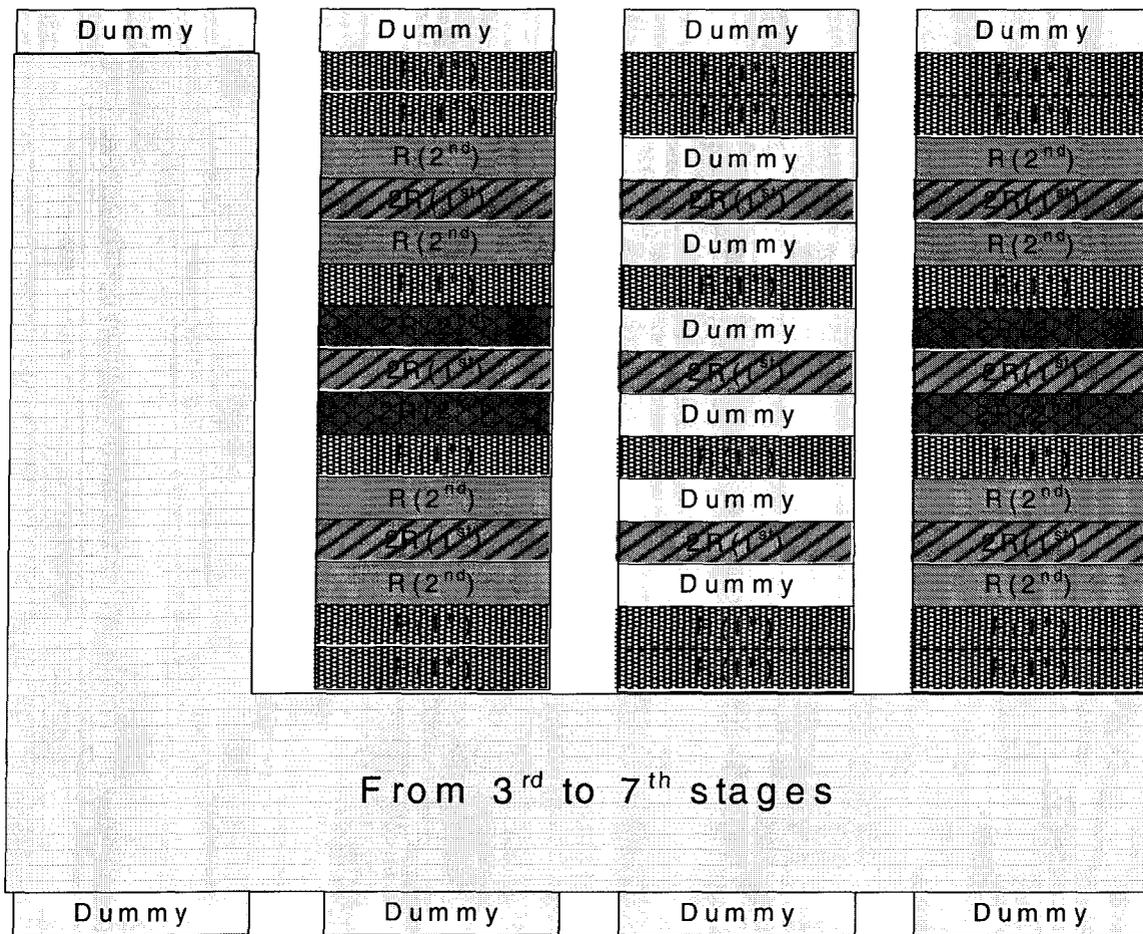


Fig. 11 Common-centroid layout of 8 bit equal-current R-2R DAC with optimal area allocation

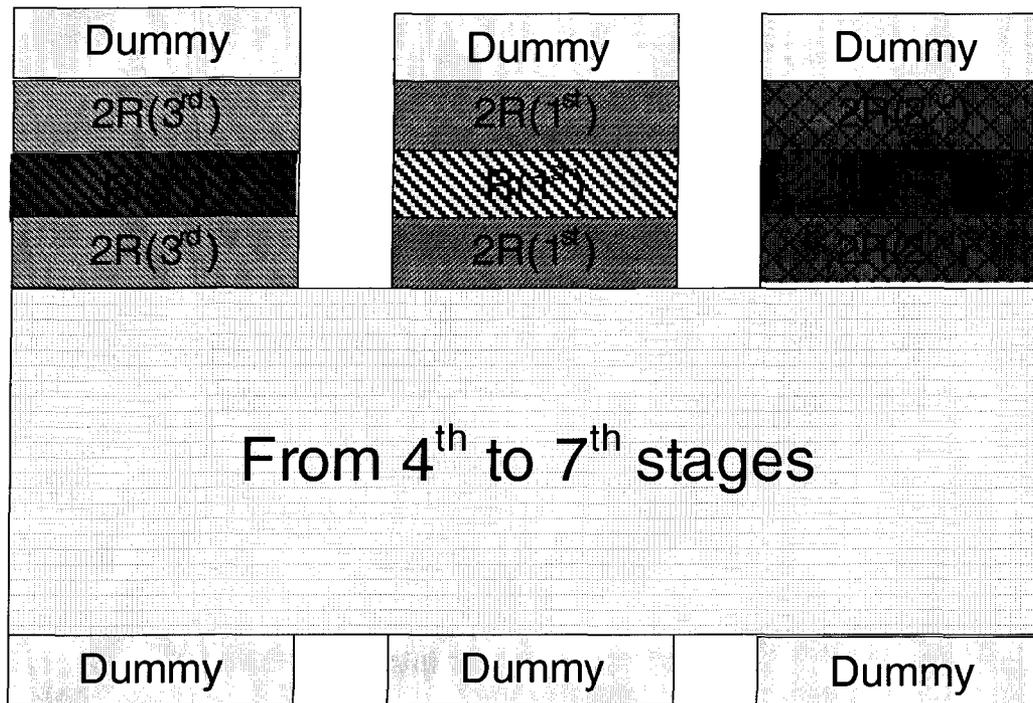


Fig.12 Common-centroid layout of 8 bit equal-current R-2R DAC with conventional series area allocation

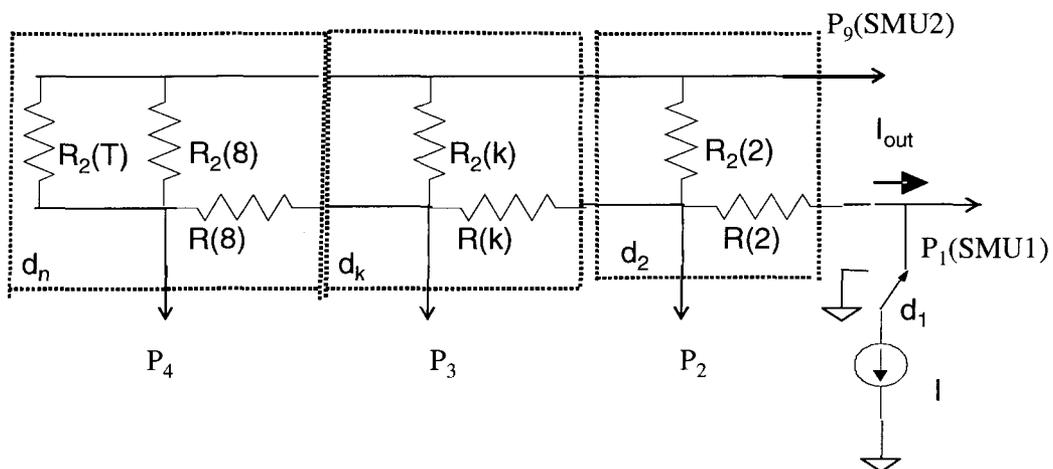


Fig.13. Schematic of 8 bit equal-current R-2R DAC with only 4 MSB stages

CHAPTER 5. KT/C CONSTRAINED OPTIMIZATION OF POWER IN PIPELINE ADCS

A paper published in *IEEE International Symposium on Circuits and Systems*

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Abstract

This paper presents a method to optimize the power consumption of a pipelined ADC with kT/C noise constraint. The total power dependence on capacitor scaling and stage resolution is investigated. With eight different capacitor scaling functions, near-optimal solution can be obtained. For 12bit pipeline ADC, the power decreases with effective number of bits per stage. This method can be easily extended to other resolution pipeline ADCs.

I. Introduction

Reducing power dissipation is very important for portable battery powered devices such as digital cameras, cell phones, laptop PCs, etc. The analog to digital data converter (ADC) is one of the most commonly used building blocks of analog and mixed signal circuits used in such devices. Video-rate applications require a high resolution, high speed ADC. The pipeline ADC [1-5] is very attractive from both aspects.

The design of an ADC involves many issues related to specific requirements such as integral nonlinearity (INL), signal to noise ratio (SNR), voltage supply, data conversion range, etc. Lewis [1] examined the stage resolution effects on area and power assuming that power ratio between the sample and hold amplifier (SHA) and comparator is constant, which

does not hold for different comparator and multiplying digital-to-analog converter (MDAC) architectures. The author concluded that minimizing the stage resolution minimizes the power dissipation. As suggested by Cline [2], low resolution pipelines favors low resolution per stage and slow capacitor scaling, which is defined as the capacitance ratio of the previous stage and the following stage, and high resolution pipelines favors high resolution per stage and rapid capacitor scaling. However, the approximation of linear relationship between the total capacitance and the total power is crude. Goes [6] gave a few design examples and concluded that the conventional wisdom of the use of the lowest possible stage resolution only applied to ADC with less than 10 bit resolution. Later on, Kwok [7] investigated the optimal stage resolution dependency of the power ratio of SHA to comparator for ADC to optimize power. It was suggested that for low power ratio of SHA and comparator less than 20, the optimal resolution is around 2 bit per stage (bps) with one bit redundancy. If the ratio is from 20~100, the optimal resolution stage will be 3 bps with one bit redundancy. For the same power ratio, high resolution pipeline ADCs favor low resolution per stage, which conflicts with the conclusion drawn by Cline [2]. Kwok also scaled the stage resolution to optimize the power. If the resolution of the ADC changes, the optimal combination of stage resolutions may change, which indicate that the results may not be applicable to different resolution ADCs.

In this paper, the strategy for power optimization with kT/C constraint will be developed. For a given total number of pipeline ADC bits, eight different capacitor scaling schemes are investigated. For each scheme, optimized power will be found with respect to effective number of bps.

II. Power Optimization

A. Power Consumption Sources

The block diagram of an h -stage m -bit/stage pipelined ADC is shown in Fig. 1. The individual stage is shown in Fig. 2. Each stage consists of a sample and hold circuit (S/H), an m -bit sub-ADC, an m -bit DAC and a switch capacitor amplifier. The blocks contained within the dashed rectangle are implemented with a single switch-capacitor circuit [2, 4] referred to as MDAC.

Each individual stage produces an m -bit binary code including one bit of redundancy. Therefore, the effective number of bits per stage is $m-1$ and the amplifier gain of the stage corresponds to this effective number of bits, i.e. for k^{th} stage the gain is given by $A_k = 2^{m-1}$. After the digital correction, the final resolution of the pipeline ADC will be $n=h(m-1)+1$.

For better performance of ADC, higher power consumption is required in the front end S/H. In a pipelined architecture, the first MDAC block can perform the function of a S/H and effectively reduces the overall power dissipation [3,5,8-10].

Without this front-end S/H, the sampling function and quantization function, i.e. MDAC and sub-ADC respectively, will be the dominant power contributor blocks for a high speed and high resolution pipeline ADC[4]. The bias circuits, calibration circuits and other auxiliary circuits also contribute to the overall power but their contribution is small compared to the pipeline stages. Further, quantization function block power dissipation can be reduced by using dynamic comparator along with redundancy and digital correction [5, 11], eliminating the need to include it in the following analysis. Under these above mentioned condition, the sampling function block will be the bottleneck in the power minimization

problem. The sampling function is mainly limited by the kT/C noise [4], which is related to the capacitor load and settling requirement of the amplifier, i.e., function of capacitor scaling and stage resolution [2].

B. Power Analysis of Pipeline Stages

As mentioned in Section II-A, capacitor scaling plays important role in overall power consumption. If the capacitors are not scaled from one stage to the next, the power of each stage will be the same and hence the total power will be large. Also, for large scaling factor, the total power consumption will be large [2]. Therefore, for optimized power, optimal scaling factor and optimal stage resolution have to be determined.

To simplify the problem, stage resolution will not be scaled. For the MDAC, which consists of switch capacitor amplifier, Fig.3, neglecting the DAC input will not change the analysis. During the phase φ_2 , the feedback factor of the k^{th} stage switch capacitor amplifier of Fig.3 is given by

$$\beta_k = \frac{C_{fk}}{C_{uk} + C_{fk}} \quad (1)$$

For the switch capacitor amplifier during phase φ_2 , the input referred RMS sampling noise voltage is given by

$$V_{rms,k} = \sqrt{\frac{kT}{C_{xk}}} \quad (2)$$

where C_{xk} is defined as the sampling capacitor for the k^{th} stage and is given by

$$C_{xk} = C_{uk} + C_{fk} \quad (3)$$

Consider a simple model of opamp, Fig. 4, modeled with a transconductance gain of g_{mk} and an output conductance of g_{ok} . The load $C_{x,k+1}$ represents the input capacitance to the next stage during the phase φ_1 . The capacitor C_{uk} will be connected to DAC output. For a multi-bit per stage architectures, C_{uk} may be comprised of several capacitors in parallel, each connected to different DAC outputs.

The gain and the gain bandwidth product of the amplifier are given by

$$A_{0k} = \frac{g_{mk}}{g_{ok}}, \quad GB_k = \frac{g_{mk}}{C_{x,k+1} + C_{uk} \beta_k (1 - \beta_k)} \quad (4)$$

The magnitude of the closed loop pole is given by

$$P_{CLk} = \beta_k GB_k \quad (5)$$

It can be shown that the time required to settle to 1/4 LSB at the k^{th} stage is given by

$$t_{sk} = \frac{\ln 2 \left(n + 2 - \sum_{i=1}^k m_i \right)}{P_{CLk}} = \frac{\ln 2 \left(n + 2 - \sum_{i=1}^k m_i \right)}{\beta_k GB_k} \quad (6)$$

where m_i is the effective number of bits per stage.

Assume now that the sampling noise contribution of stage k , referred back to the input, is given by

$$V_{rmseq,k} = \lambda_k \sqrt{\frac{kT}{C_{x1}}} \quad (7)$$

where λ_k relates the input referred kT/C noise of k^{th} stage to that of the total capacitance of the first stage and hence $\lambda_1 = 1$. Since each of these noise sources is uncorrelated, it follows that the input referred RMS noise voltage due to all h stages is given by

$$V_{rms} = \sqrt{\frac{kT}{C_{x1}}} \sqrt{\sum_{k=1}^h \lambda_k^2} \quad (8)$$

For acceptable noise budget of x bit below the ADC resolution, i.e.

$$V_{rms} = \frac{V_{LSB}}{2^x} \text{ with } V_{LSB} = \frac{V_{REF}}{2^n} \quad (9)$$

The total 1st stage capacitance from (8) and (9) is given by

$$C_{x1} = kT \frac{2^{2(n+x)}}{V_{REF}^2} \sum_{k=1}^h \lambda_k^2 \quad (10)$$

For $k > 1$, the noise of k^{th} stage referred back to the input of the pipeline is given by

$$V_{nrmsseq\ k} = \frac{1}{\prod_{i=1}^{k-1} 2^{m_i}} V_{rms,k} = \frac{1}{2^{\sum_{i=1}^{k-1} m_i}} V_{rms,k} \quad (11)$$

It follows from (2), (7), and (11) that

$$\lambda_k = \sqrt{\frac{C_{x1}}{C_{xk}}} \cdot \frac{1}{2^{\sum_{i=1}^{k-1} m_i}} \quad (12)$$

This can be solved for C_{xk} to obtain

$$C_{xk} = \frac{C_{x1}}{2^{\sum_{i=1}^{k-1} m_i} \lambda_k^2} \quad (13)$$

The transconductance gain of the amplifier is given by

$$g_m = \theta \frac{2I_Q}{V_{EB}} \quad (14)$$

where I_Q is the total quiescent current of the amplifier, V_{EB} is its excess bias of the input device, and θ is an architecture-dependent power efficiency penalty factor for the amplifier. It can be assumed that θ is independent of the port electrical variables of the amplifier, and $\theta \leq 1$. For a single-stage single-ended amplifier, $\theta = 1$. From (4), (6) and (14), the quiescent current of stage k is given by

$$I_{Qk} = \frac{C_{xk}\beta_k(1-\beta_k) + C_{x,k+1}}{2\beta_k t_{sk}\theta_k} V_{EBk} \left(n + 2 - \sum_{i=1}^k m_i \right) \ln 2 \quad (15)$$

The total power dissipation in the ADC is given by

$$P = V_{DD} \sum_{k=1}^h I_{Qk} \quad (16)$$

Consider the special case where all stages are identical (for all k , $m_k = m$, $\beta_k = \beta$, $\theta_k = \theta$, and $t_{sk} = t_s$). This case will be used as a baseline for comparison. It follows from (12) that

$$C_{xk} = \frac{C_{x1}}{2^{2m(k-1)} \lambda_k^2} \quad (17)$$

with $\beta = \frac{1}{2^m}$, Equation (17) can be substituted into (15) to obtain

$$P = \left[\frac{V_{DD} V_{EB} kT \ln 2}{2t_s \theta V_{REF}^2} 2^{2x} \right] \left[2^{2n+m} \right] \left[\sum_{k=1}^h \lambda_k^2 \right] \sum_{k=1}^h \left(\frac{n+2-km}{2^{2km}} \left(\frac{2^m-1}{\lambda_k^2} + \frac{1}{\lambda_{k+1}^2} \right) \right) \quad (18)$$

Further, the first term in brackets on the right hand side of (18) can be normalized out since it is not a function of m , n or the λ variables. Thus, we will define the normalized power by the expression

$$P_{NORM} = \left[2^{2n+m} \right] \left[\sum_{k=1}^h \lambda_k^2 \right] \sum_{k=1}^h \left(\frac{n+2-km}{2^{2km}} \left(\frac{2^m-1}{\lambda_k^2} + \frac{1}{\lambda_{k+1}^2} \right) \right) \quad (19)$$

III. Results

From (19), we know that the optimization of the power for a given pipelined ADC involves determining m and λ_k variables for given values of n and x . Therefore, the total number of variable will be around $h+1$. In order to reduce the design variables, we examined eight different capacitor scaling functions. The 8 different capacitor-scaling functions are given below:

- 1) Equal stage noise ($\lambda_k = 1$)

$$P_{NORM} = \left[2^{2n+m} \right] h \sum_{k=1}^h \left(\frac{n+2-km}{2^{(2k-1)m}} \right) \quad (20)$$

- 2) Noise Dominated by 1st stage ($\lambda_k = 1, \lambda_k = 0.1$)

$$P_{NORM} \cong \left[2^{2n+m} \right] \left[1 + \frac{h-1}{100} \right] \left[\frac{n+2-m}{2^{2m}} (2^m + 99) + \sum_{k=2}^h \left(\frac{n+2-km}{2^{2km}} 100(2^m) \right) \right] \quad (21)$$

- 3) First stage provides approximately half of the noise ($\lambda_k^2 = \frac{1}{2^{k-1}}$)

$$P_{NORM} = \left[2^{2n+m} \right] \left[2 - \frac{1}{2^{h-1}} \right] \sum_{k=1}^h \left(\frac{n+2-km}{2^{2km}} (2^{k-1} (1 + 2^m)) \right) \quad (22)$$

- 4) First stage provides more gain ($\lambda_k^2 = \frac{1}{2^{z(k-1)}}$, where z is a constant)

$$P_{NORM} = \left[2^{2n+m} \right] \left[\sum_{k=1}^h \frac{1}{2^{z(k-1)}} \right] \sum_{k=1}^h \left(\frac{n+2-km}{2^{2km}} (2^{z(k-1)} (2^m + 2^z - 1)) \right) \quad (23)$$

- 5) First stage provides more gain ($\lambda_k^2 = \frac{1}{2^{zn(k-1)}}$ where z is a constant)

$$P_{NORM} = [2^{2n+m}] \left[\sum_{k=1}^h \frac{1}{2^{2m(k-1)}} \right] \sum_{k=1}^{h-1} \left(\frac{n+2-km}{2^{2km}} (2^{2m(k-1)} (2^m + 2^{2m} - 1)) \right) \quad (24)$$

6) First stage provides more gain ($\lambda_k^2 = \frac{1}{2^{z\sqrt{k-1}}}$ where z is a constant)

$$P_{NORM} = [2^{2n+m}] \left[\sum_{k=1}^h \frac{1}{2^{z\sqrt{k-1}}} \right] \sum_{k=1}^h \left(\frac{n+2-km}{2^{2km}} (2^{z\sqrt{k-1}} (2^m - 1) + 2^{z\sqrt{k}}) \right) \quad (25)$$

7) First stage provides more gain ($\lambda_k^2 = \frac{1}{2^{2m\sqrt{k-1}}}$ where z is a constant.)

$$P_{NORM} = [2^{2n+m}] \left[\sum_{k=1}^h \frac{1}{2^{2m\sqrt{k-1}}} \right] \sum_{k=1}^h \left(\frac{n+2-km}{2^{2km}} (2^{2m\sqrt{k-1}} (2^m - 1) + 2^{2m\sqrt{k}}) \right) \quad (26)$$

8) First stage provides more gain ($\lambda_k^2 = z\lambda_{k-1}^2$, where z is a constant)

$$P_{NORM} = [2^{2n+m}] \frac{1-z^h}{1-z} \sum_{k=1}^h \left(\frac{n+2-km}{2^{2km}} \left(\frac{2^m-1}{z^{k-1}} + \frac{1}{z^k} \right) \right) \quad (27)$$

For 12 bit ADC, numerical computation showed that case 4 with $z = \sqrt{2}$, case 5 with $z = \sqrt{\frac{1}{2}}$, and case 8 with $z=0.38$ have the best power performances as shown in Table 1. The other cases have much poorer performance, and are not shown here. From the results, it was observed that when m increases, the power decreases.

The optimal value of m is also going to be a function of ADC specifications. If the data conversion range is very small, then the offset of dynamic comparator will cause problems with the over-range protection of the ADC. To overcome this problem we have to use a static comparator and then the power consumption of the comparator cannot be ignored. Depending on the design of comparator, the optimal value of m can be 2, 3 or 4. Typical values of dynamic comparator offset can be easily few tens of mV[12]. If a 2V pipelined ADC implemented in a 0.18 um process has a maximum signal swing of only 1V,

it may be more reasonable to have 2 effective-bits/stages instead of 4 to ensure adequate room for over-range protection.

TABLE I. THE POWER AND CAPACITANCE OF PIPELINE ADC

Effective bps	Normalized Overall Power and Capacitance					
	<i>Case 4</i> <i>with $z=1.414$</i>		<i>Case5</i> <i>with $z=0.707$</i>		<i>Case8 with</i> <i>$z=0.38$</i>	
m	Power	Cap	Power	Cap	Power	Cap
2	31.463	1.915	31.463	1.915	31.449	1.925
3	21.497	1.637	21.251	1.389	21.557	1.647
4	16.843	1.532	16.302	1.194	16.902	1.540

IV. Conclusions

A method to optimize the power with kT/C noise constraint was proposed. Eight different scaling schemes were investigated to achieve near optimal solution. It was shown that for a 12 bit ADC, the total power decreases with the stage resolution provided comparator consumption is neglected. Although, the computation was done for a 12-bit ADC, the method can be easily extended to other resolution pipeline ADCs.

In this paper, only capacitor scaling was considered. Further study is needed to incorporate stage resolution scaling into the present capacitor scaling scheme for better understanding of the power optimized solution of a pipeline ADC.

Acknowledgement

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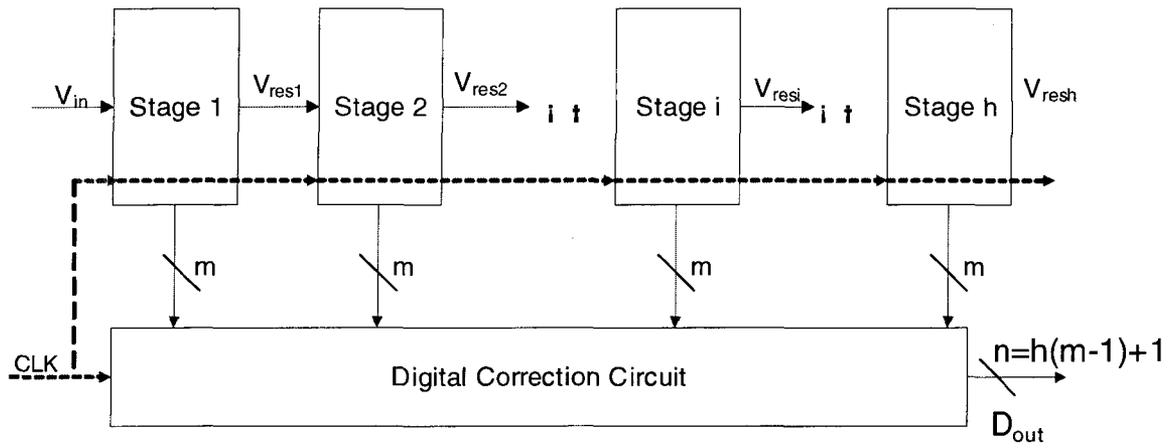


Fig. 1 Basic pipelined data converter architectures

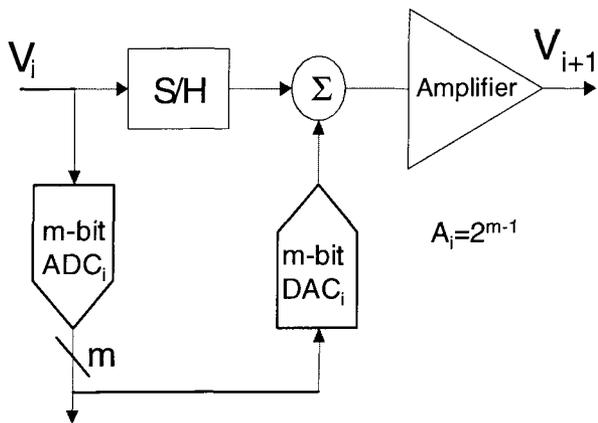


Fig.2. k^{th} Stage of basic pipelined data converters

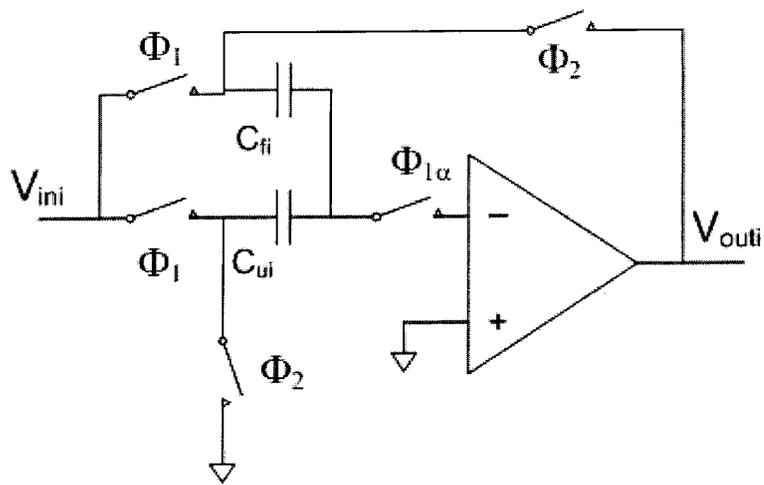
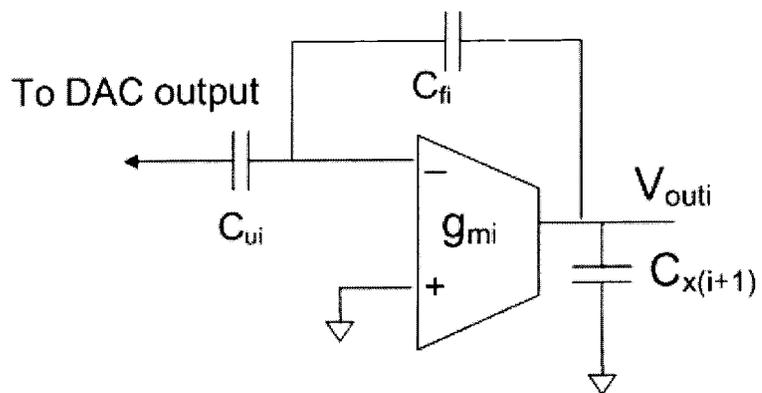
Fig.3 k^{th} MDAC

Fig.4 Operational amplifier of each stage

CHAPTER 6. NEW OVER-RANGE PROTECTION SCHEME IN PIPELINED DATA CONVERTERS

A paper published in *IEEE Midwest Symposium on Circuits and Systems*

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Abstract

Existing approaches for the design of interstage switched-capacitor amplifiers used in pipelined data converters have evolved following the notion that there are firm limits on input range and output range of the amplifier. In this work, it is recognized that the limits on signal swing are not dictated by binary and somewhat arbitrary boundaries but rather by increasing levels of distortion with signal swing. The concept of defining a series of signal swing windows based on the degree of distortion present in the gain stage amplifier is formalized. A set of "critical points" on the transfer characteristics are identified that are useful for determining robustness of any given over-range protection circuit. In contrast to existing approaches where the amplifier may be under-designed or over-designed in an attempt to meet a fixed signal swing window requirement, the designer can select signal swing windows to provide acceptable levels of distortion. Following this approach, a new over-range protection scheme is developed which ensures that all residues of a given stage are mapped back into an acceptable distortion window of the following stage

I. Introduction

The presence of uncompensated nonlinearities in the signal path can significantly degrade the performance of a pipeline analog to digital converter (ADC). Few of these nonlinearities contribute to recoverable errors whereas other results in non-recoverable errors. Recoverable errors may cause an error in the overall interpretation of the digital output code, but sufficient information still exists in the digital output for correct interpretation. In contrast, non-recoverable errors cause a loss of information and sufficient information does not exist for the recovery. Both non-recovered recoverable errors and non-recoverable errors limit the performance of most pipeline data converters. Excessive growth in the residue path caused by nonlinearities will cause such recoverable or non-recoverable errors. In particular, the concern is that the residue can cause the output of one or more amplifier stages to saturate. These excessive signals are often termed over-range signals. Modifications of the basic amplifier structure are included in some pipeline ADCs [1-4] to limit the over-range signals. The circuits that provide this over-range protection are generally termed an over-range protection circuits.

Common practice for over-range protection circuits is to use the same signal conversion range for all the stages. Moreover, no distinction is made between the signal conversion range and signal saturation range [1-4]. This results in excessive design requirements of a pipeline ADC. To overcome this problem, a series of signal swing windows based on the degree of distortion present in the gain stage amplifier is formalized. A set of "critical points" on the transfer characteristics are identified that are useful for determining robustness of any given over-range protection circuit. A new over-range

protection scheme based on these signal swing windows and critical points will be investigated to achieve a relaxed pipeline ADC design.

II. Linearity and Over-ranging

A. Operating Windows

Consider the signal path from the input to the output of a stage of pipeline ADC as depicted in Fig. 1. The two-dimensional input/output plane in Fig. 2 shows the normal input and output operating range of the amplifiers for an arbitrary amplifier stage relative to the reference range of the ADC. In Fig. 2, V_{DD} and V_{SS} represent the upper and lower supply voltages. It is generally assumed that it is necessary to keep the input and output in a rectangular window positioned on $V_{in}=V_{out}$ line. This window is defined as Data Converter Reference Window (DCRW) and it is the inner most rectangle shown in Fig.2. For convenience, it will be assumed that the position of the DCRW is the same for all stages. The specified input range of the ADC corresponds to the projection of the DCRW onto the V_{in} axis. Another important window can be defined as Residue Amplifier Saturation Window (RASW). This window is determined by few devices internal to the op-amp leaving the desired region of operation and causing amplifier to saturate. If the signal is out of the RASW range, serious non-recoverable distortion or clipping will result in the amplifier. Besides, there exists another window in between DCRW and RASW, Residue Amplifier Distortion Window (RADW). Outside this RADW window, distortion or nonlinearities becomes larger than the tolerable limit for the overall feedback amplifier (not just the operational amplifier) for a given pipeline stage. Within the RADW and RASW, the distortion can actually be reduced by calibration. The RADW is depicted as a rectangle in

Fig. 2, but in actuality, this may be arbitrarily-shaped. This distortion bound has not been sufficiently studied and has not been considered for the design issues.

In most reported designs, no distinction is made between the DCRW and the RASW [1-4]. For an n -stage pipeline ADC, it is generally further assumed that it is necessary to keep the input and output signals inside the DCRW for all stages. This type of overage-protection scheme is far from necessary. In what follows, we propose linearity and over range protection method to relax the requirement based on the discussion of the concept of windows.

Fig. 3 shows the combined effects of several error sources in one of the first $(n-2)$ stages of a pipeline ADC. Since the last stage of a pipeline ADC comprised of only a comparator, the $(n-1)^{\text{th}}$ stage output should be bounded by DCRW otherwise the last stage error can not be corrected. This is equivalent to having over-range protection on the $(n-1)^{\text{th}}$ stage. Whereas, for the first $(n-2)$ stages, the input and output are only required to lie within the RADW window. In case (a), the amplifier is driven to the RADW. In case (b), modest distortion will occur as the output leaves the RADW window. This will cause degradation in the performance of the pipeline. Actually, this type of error may be correctable with the appropriate nonlinear error correction algorithm but very little is available in the literature on these corrections. The third situation, case (c), corresponds to impinging on the RASW. This will cause serious distortion and non-recoverable errors in the pipeline.

To correctly convert the input voltage, a less stringent but still sufficient condition would be to have linearity protection circuitry on the amplifiers of the first $(n-2)$ stages and over-range protection on the $(n-1)^{\text{th}}$ stage, i.e.:

- 1) The input and output signals for the first $(n-2)$ stages must lie within the RADW

- 2) The output range for the $(n-1)^{\text{th}}$ stage must lie within the DCRW

These conditions must be maintained for all specified input signals and throughout all process and temperature variations. It should be noted that the issue of over range plays no role on any stage except the output of the $(n-1)^{\text{th}}$ stage provided that the previous stages amplifier remain linear. Of course, many designers use over-ranging to maintain linearity on intermediate stages as well. One of the major reasons that many existing data converters fail to meet static linearity constraints is associated with improper sizing of the DCRW and the RADW. This may be a challenge because creating a large RADW, specifically large enough to contain the DCRW, can be difficult.

B. Critical Points

Some points on the transfer characteristics of a residue amplifier that are particularly indicative of non-idealities in the pipeline stage can be defined as Critical Points (CP). These points must be constrained to prevent the amplifier from saturating to avoid non-recoverable errors. The vulnerability of the amplifier is due to the fact that the non-idealities in the amplifier cause these points to move. The movement of these points from their ideal locations can be an indicator of degradation in performance of the pipeline. For a 1-bit per stage pipeline, the critical points are shown by the circles in Fig. 4. The radius of the circles will be used to identify the worst-case deviation of these critical points from their desired values due to non-idealities in the circuit. These CPs can be further classified as Internal Critical Points (ICP) or Boundary Critical Points (BCP). The ICPs are the points where discontinuities of the ideal transfer characteristic occur, which are close to or beyond the DCRW, e.g. points B in Fig. 4. The BCPs are the points corresponding to the minimum and

maximum input of a stage which are close to or beyond a horizontal DCRW boundary, e.g. points D in Fig. 4. The points with the worst case deviation that remain within the DCRW will not be termed as CPs.

BCPs that are near a vertical edge of DCRW are problematic for two reasons. First, if the output of the previous stage, i.e. the input of the present stage, extends beyond the DCRW boundary, the output of this stage may go beyond the RADW. Second, the movement of these points can also affect both the output range of the present stage and the input of the next stage. The ICPs affect the output range of the stage and may also affect the distortion.

In the next section we will identify a new window based on CPs and propose an over-range protection scheme where the CPs will not cause problems.

III. Strategies for Providing Over-Range Protection

In this discussion, we will focus on the operation of a pipeline stage in the range of the DCRW. Fig. 5 shows the transfer characteristics of an ideal 1-bit/stage architecture including the unity gain line. It can be observed that the unity gain line crosses the transfer characteristics of the amplifier at the two corners of the DCRW and there are two ICPs and BCPs. This does not necessarily suggest that this architecture should be avoided, but rather indicates that the accurate control of the variation will be essential for good yield. Good yield will be increasingly difficult to achieve as the resolution of the ADC increases.

The previous examples provided insight into the properties that are needed to develop a new linearity and over range protection scheme, which is termed as new over-range protection scheme.

A. Critical Window

The concept of critical window (CW) based on the DCRW, RADW and the transfer characteristic is defined below.

Fig.6 shows CW for 3 different cases. The 1st vertical CW edge is defined by the intersection of 1st transfer curve segment with that of the lower horizontal line of the DCRW, whereas, for 2nd vertical CW edge is defined by last transfer curve segment with that of the upper horizontal line of the DCRW. The horizontal lines of the CW are same as those of the DCRW. For instance, if we have 2 BCPs, e.g., case (b), the CW will be a subset of DCRW. For case I and case II, the RADW is outside of CW. For case III, part of RADW is inside of CW, and a new critical window (NCW) is defined by the innermost closure of these two windows.

For simplicity, we will assume that the DCRW is the same for all the stages, but the RADW can be different from stage to stage. It is also assumed that CW can be inside of the DCRW or outside of the DCRW. The detailed design strategy for new over-range protection scheme based on the signal swing windows and CPs is shown in Fig.7, along with the linearity and over-range protection scheme discussed in II-A.

The main idea of this strategy is to insure the residue of each stage is mapped back into an acceptable distortion window of the following stage. For example, if stage k is of case I or II and stage $(k+1)$ is of case II, and if there is any CP present in stage k , it would result in the output of stage k to exceed the CW_k . This will cause signal to become larger than the input range of the stage $(k+1)$ and cause non recoverable errors.

IV. Conclusions

A new scheme for over-range protection for a pipeline ADC was proposed. Concepts of a series of signal swing windows, i.e., Data Converter Reference Window (DCRW), Residue Amplifier Saturation Window (RASW) and Residue Amplifier Distortion Window (RADW) were formalized. A set of critical points (Cps), i.e. Boundary Critical Points (BCP) and Internal Critical Points (ICP) were identified based on the signal swing windows. In contrast to existing approaches which attempt to meet a fixed signal swing window, this new scheme provides flexibility for designers to choose different signal swing windows. A Critical Window (CW) and New Critical Window (NCW) based on different combinations of the above mentioned windows and CPs were identified. A design strategy for the new over-range protection scheme was developed and shown in the flow chart.

Acknowledgement

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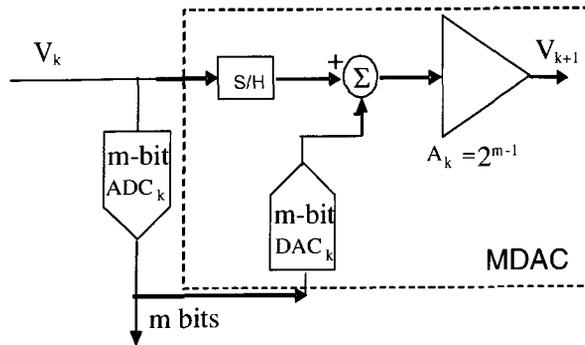


Fig. 1 Block diagram of k^{th} stage of pipeline ADC

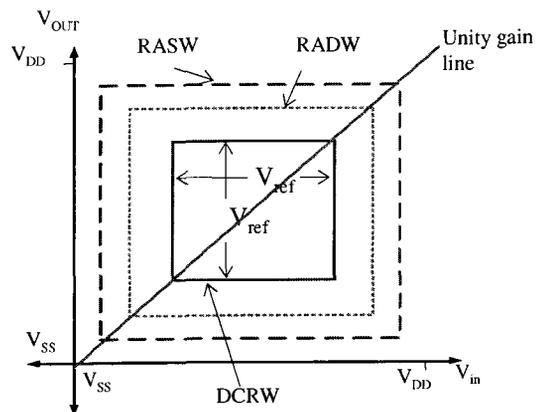
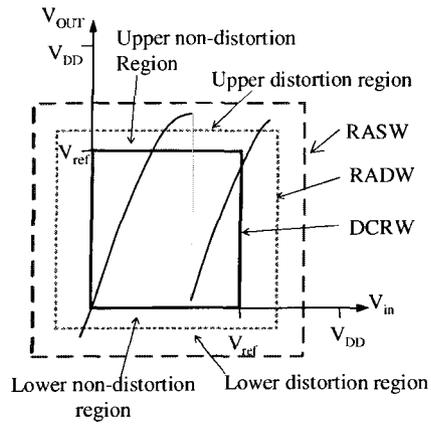
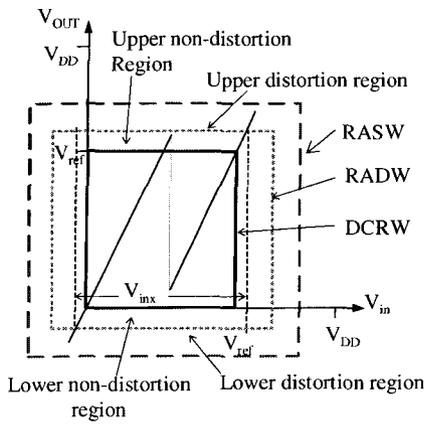


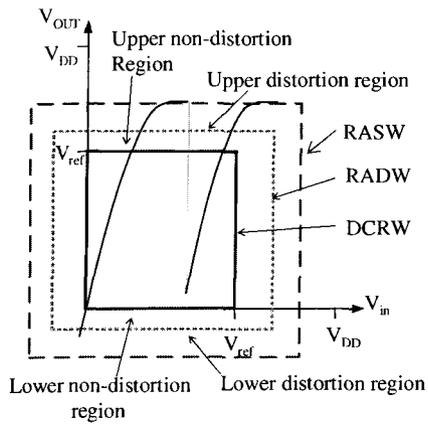
Fig. 2 Input/Output range of amplifier stage in pipelined ADC



(a)



(b)



(c)

Fig. 3 Effects of driving residue amplifier beyond the DCRW

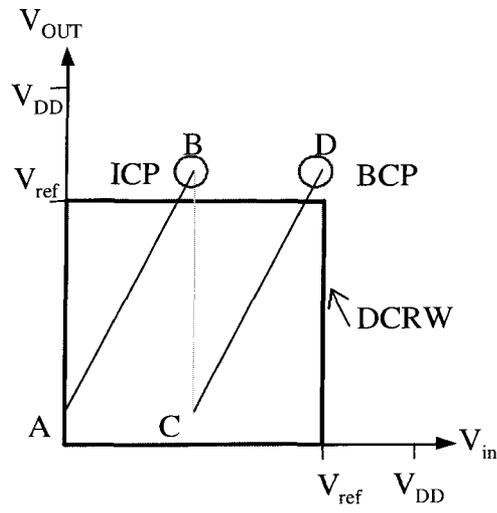


Fig. 4 Critical points for one-bit per stage amplifier

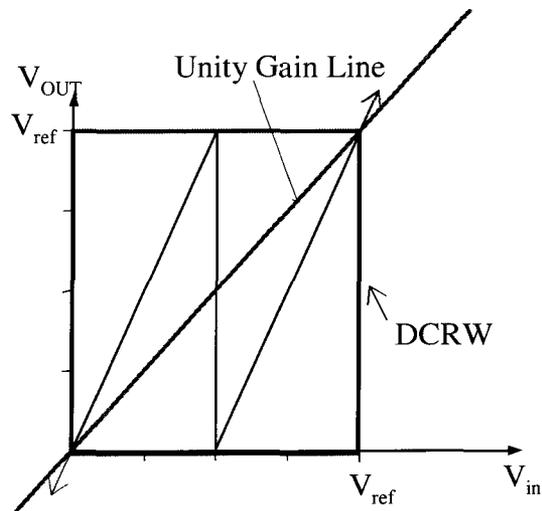
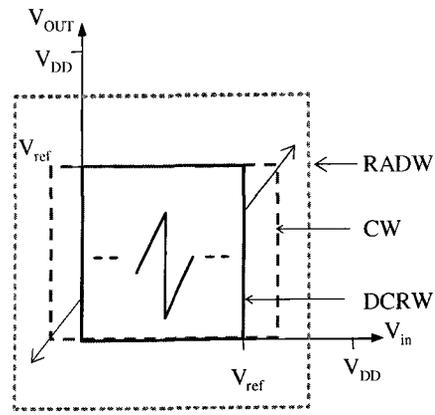
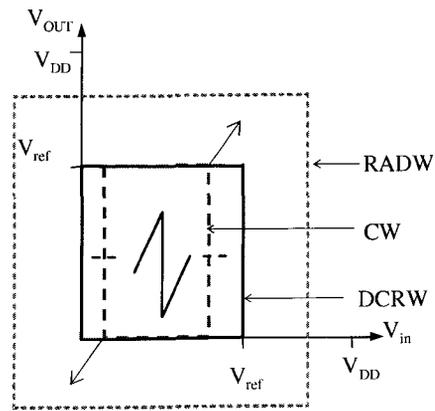


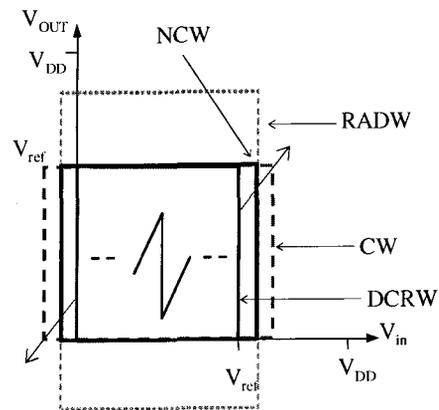
Fig. 5 Single bit/stage structure showing over-range sensitive region



(a)



(b)



(c)

Fig. 6 (a) case I (b) case II (c) case III for CW

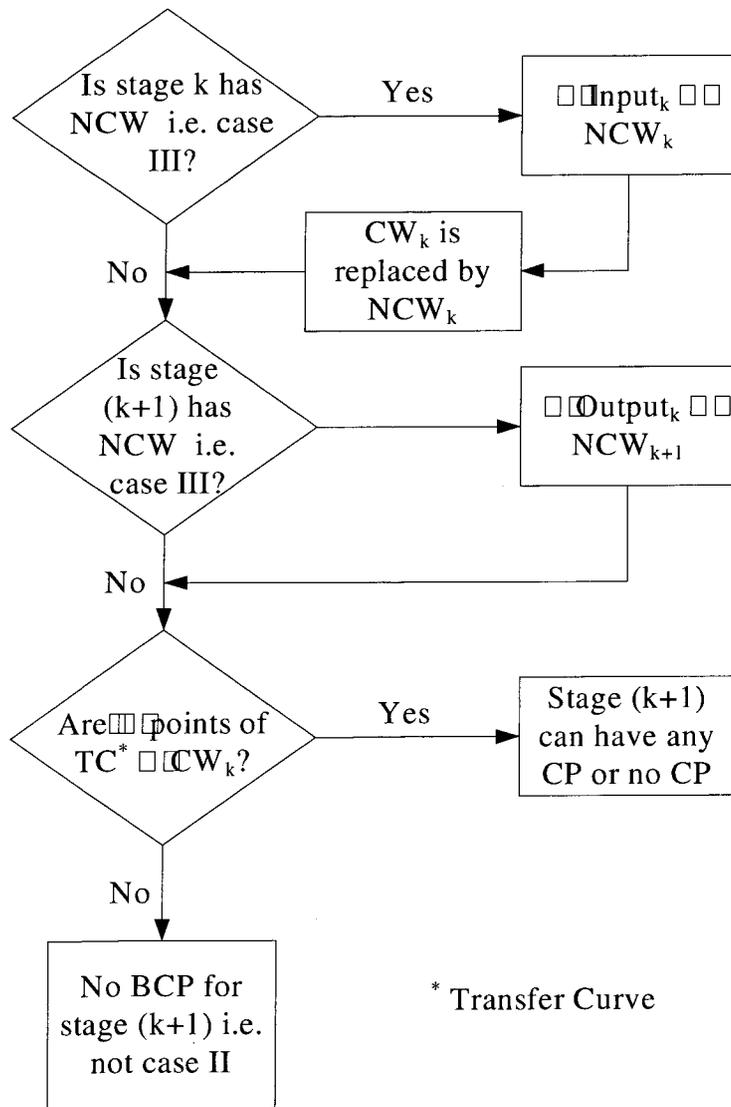


Fig. 7 Flow chart for new over-range protection scheme

CHAPTER 7. GENERAL CONCLUSIONS

With the continued down-scaling of semiconductor process, random variations of process parameters are adversely affecting the performance of matching-critical analog circuits in increasingly significant ways.

Existing approaches for managing production costs of matching-critical circuits have mainly focused on improving yield by increasing the area of the matching-critical components. Unfortunately, it is recognized that a high yield does not always guarantee low production costs. This work shows that without increasing the circuit area, the performance and yield of matching-critical analog circuits can be improved without increasing the production costs. Optimal and near-optimal area allocation strategies are proposed for rationed resistors, resistive feedback amplifiers, and R-2R DACs. These techniques can provide significant improvement of yield when compared to conventional area allocation approaches for fixed total resistor area. It is also shown that even for the same functional block, the optimal area allocation scheme can be different if used in different applications. Although the focus in this work is on area allocation for integrated film resistors, the contents can be applied to other matching-critical circuits where matching of transistors or capacitors is of primary concern.

The number of bits per stages (bps) and capacitor sizing are two important design parameters for pipeline ADC design. However, the literature provides mixed ideas about the optimal bps and capacitor sizing. In this dissertation, a strategy to optimize the power consumption in a class of digitally calibrated pipelined ADCs with a kT/C noise constraint is proposed. Optimal bps and capacitor scaling strategies are introduced. It is shown that

significant reductions in total power consumption can be achieved with optimal noise distribution and bps allocation.

Existing approaches for the design of interstage switched-capacitor amplifiers used in pipelined data converters have evolved following the notion that there are firm limits on input range and output range of the amplifier. This often results in excessive design requirements of a pipeline ADC. In this dissertation, a new over-range protection scheme based on identifying signal swing windows is developed. This approach can be used to ensure that all residues of a given stage are mapped back into an acceptable distortion window of the following stage. With this approach, performance requirements of the operational amplifiers used in pipeline ADC designs can be relaxed.